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A low-voltage and energy-efficient full adder cell based on carbon nanotube technology

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Scaling problems and limitations of conventional silicon transistors have led the designers to exploit novel nano-technologies. One of the most promising and feasible nano-technologies is CNT (Carbon Nanotube) based transistors. In this paper, a high-speed and energy-efficient CNFET (Carbon Nanotube Field Effect Transistor) based Full Adder cell is proposed for nanotechnology. This design is simulated in various supply voltages, frequencies and load capacitors using HSPICE circuit simulator. Significant improvement is achieved in terms of speed and PDP (Power-Delay-Product) in comparison with other classical and state-of-the-art CMOS and CNFET-based designs, existing in the literature. The proposed Full Adder can also drive large load capacitance and works properly in low supply voltages.

Keywords: CNFET; Low-Voltage; Full-Adder; Minority-Function; Nanotechnology

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Scaling down the feature size of MOSFET devices in nanometer, leads to serious challenges, such as short channel effects, very high leakage power consumption and large parametric variations. Due to these limitations researchers become eager to work toward new emerging technologies such as Quantum Automata (QCA) [1], Nanowire transistors [2] and Carbon Nanotube Field Effect Transistors (CNFET) [3]. By the mentioned problems of nanoscale CMOS technology, which makes it unsuitable for low-power and low-voltage applications in the near future, these nano-devices could replace the conventional silicon MOSFET in the time to come. However, due to the similarities between the infrastructure and functionality of the conventional MOSFET devices with CNFETs and also because of the ballistic operation of CNFETs, it could be more promising and achievable, compared to other nano-devices. Recently some efforts have been done for designing circuits based on CNFET such as multiple valued logic circuits [4,5], arithmetic circuits [6] and so on, taking advantages of its unique attributes. However, among these circuits arithmetic circuits could be more interesting, due to their vast range of applications. Many VLSI systems such as microprocessors, DSP architectures and nano-micro systems [7,8,9] have arithmetic unit, which is also included in their critical path. One of the most important and basic arithmetic units is Full Adder, which could be the basic structure of many complex arithmetic systems and as a results its performance directly affects the performance of the whole system. Therefore, it is necessary to design novel Full Adder structures with higher performance and lower power consumption, based on the emerging nano technologies. In this paper a new energy-efficient 1-bit Full Adder cell is proposed, which takes advantage of CNFET devices and high density Carbon Nanotube Capacitors (CNCAP) [10]. The proposed circuit is also compared with the classical and state-of-the-art CMOS and CNFET-based Full Adders, with different styles, which are briefly introduced in this section.

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CCOM Full Adder cell [11], which has 28 transistors, is the classical CMOS Full Adder cell designed based on the conventional complementary style of design. CMOS-Bridge Full Adder cell [12], which has 24 transistors, is a state-of-the-art CMOS Full Adder cell designed based on a low-power style of design, called Bridge style. Hybrid1 [13] and Hybrid2 [14] Full Adder cells, which have 26 and 24 transistors, respectively, are composed of different high-performance 2-input XOR-XNOR circuits and hybrid CMOS style. TG Full Adder cell [15], which has 18 transistors, is the classical high-performance Full Adder cell, designed based on Transmission gates (TG). The CNT-FA-1, presented in [4] (see Fig. 1(a)), is minority function based Full Adder with 8 transistors and 7 capacitors. CNT-FA-2 presented in [5] (see Fig. 1(b)), which is composed of 12 transistors and 8 capacitors, is based on majority-not, NAND and NOR functions. A minority function is used to produce C_{out} signal. Another minority function is exerted on input capacitors and two NAND and NOR gates to implement Sum signal.

Carbon Nanotube Field Effect Transistors (CNFETs)

Carbon Nanotube (CNT), which was discovered in 1991 by S. Iijima is a nano-scale tube created by rolling sheets of graphite [16]. Recently, it has become one of the new research trends in physics, chemistry, mechanics, biology and electronics due to its outstanding properties. A CNT could be single-wall (SWCNT) or multi-wall (MWCNT), due to the number of cylinders used in its structure. A SWCNT could be metallic or semiconducting due to its chiral number (n1, n2). Chiral number defines the form of the placement of the carbon atoms along a CNT. If n_1-$n_2 \neq 3k\,(k \in Z)$, the SWCNT is semiconducting otherwise it is metallic [17]. Electronic device designers exploit semiconducting SWCNT as the channel of the Carbon Nanotube Field Effect Transistor (CNFET), which was first fabricated by Tans, Verschueren, and Dekker in 1998 [18]. CNFETs, like MOSFETs, have P-type and N-type devices. However, the great advantage of CNFET devices is that the P-type and N-type CNFETs with the same device size have the same mobility, which simplifies the process of transistor sizing, specifically in complex circuits with a large number of transistors [19]. Furthermore, CNFET based circuits are faster and have lower average power consumptions, in comparison with current MOSFET-based designs [19].

The current-voltage (I-V) characteristics of the CNFET and MOSFET devices are similar. In addition, similar to the MOSFET devices, CNFETs have threshold voltage, which is required for turning on the device. The threshold voltage of a CNFET is inversely proportional to the diameter of the CNT as it is shown in Eq. (1). This makes it possible for CNFET to be turned on, at the required voltages and therefore, designing complex circuits with better performance becomes more feasible [17].

$$V_{th} \approx \frac{E_g}{2.e} = \frac{\sqrt{3}}{3}\frac{a.V_\pi}{e.D_{CNT}} \approx \frac{0.43}{D_{CNT}(nm)}\,\mathrm{V} \qquad (1)$$

Where E_g is the band gap, V_π (≈ 3.033 eV) is the carbon

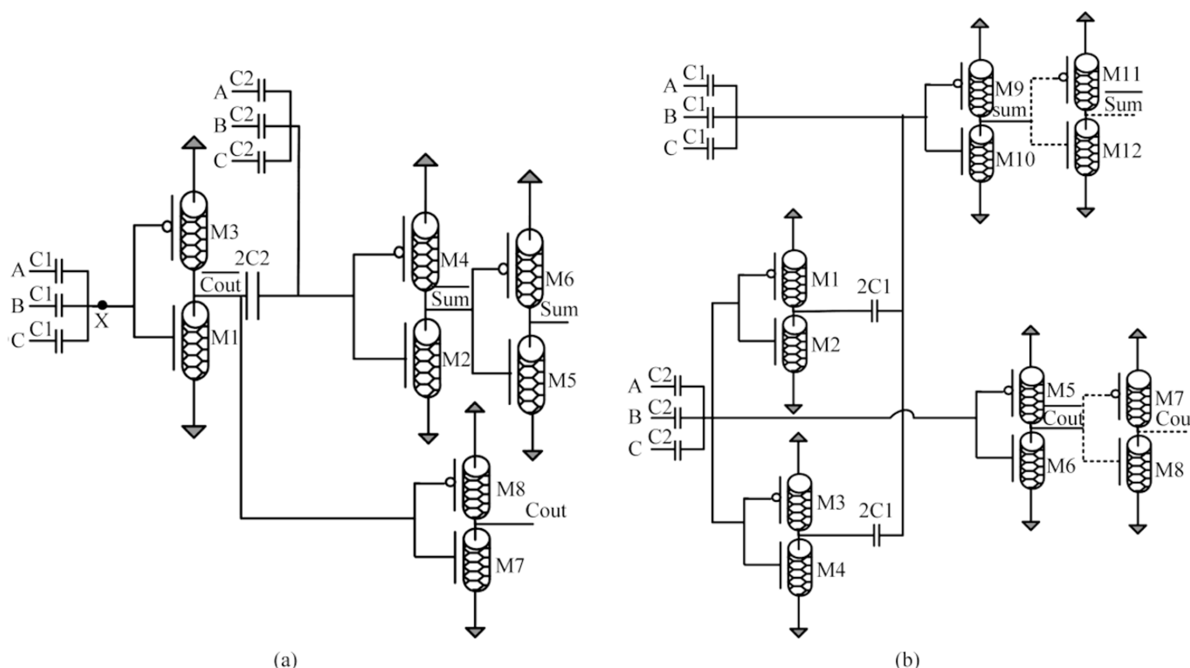


FIG.1. Previous CNFET-based works (a) CNT-FA-1 (b) CNT-FA-2.

π-π bond energy in the tight bonding model, parameter a (≈ 0.249 nm) is the carbon to carbon atom distance, e is the unit electron charge, and D_{CNT} is the diameter of CNT. D_{CNT} itself could be calculated based on the following equation [17]:

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \approx 0.078 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (2)$$

Three different types of CNFETs have been already presented in the literature. The first type is Schottky Barrier CNFET (SB-CNFET) (see Fig. 2(a)), which is composed of a metal-semiconducting nanotube-metal junction, and operates under the principle of direct tunneling by way of the Schottky barrier formed by nonideal contact between metal and carbon nanotube. The main drawback of this kind of CNFET is that the metal-nanotube contact actually limits the transconductance of the CNFET in the ON state and decreases the current delivery capability, which is a significant parameter for high speed operation in a device. In addition, strong ambipolar attributes of SB-CNFET limit the usage of this type of device in customary logic families. SB-CNFET is appropriate for medium to high-performance applications. The second type of CNFET is the band-to-band tunneling CNFET (T-CNFET) (see Fig. 2(b)) and has super cut-off characteristics and low ON currents, which makes it very appropriate for ultra-low-power and subthreshold applications but is not suitable for very high-speed applications. The third kind of CNFETs, which can make a compromise between very high-speed operation and low power consumption, is the MOSFET-like CNFET (see Fig. 2(c)). In this type of device, Potassium doped drain and source nanotube regions have been fabricated and field-effect behaviour and unipolar characteristics have been achieved. The main advantage of MOSFET-like CNFET is that its source-channel junction has no Schottky Barrier and as a result, it has significantly high ON current. Therefore, MOSFET-like CNFETs are very suitable for ultra-high-performance digital applications [3].

Based on the mentioned advantages and disadvantages of different types of CNFETs and also due to more similarities between MOSFET-like CNFETs and MOSFETs in terms of working and characteristics, in this paper MOSFET-like CNFETs are utilized for designing the proposed circuit.

Proposed Full Adder Cell

The proposed Full Adder design is implemented by means of majority function, based on carbon nanotube technology. This design is based on the idea that the C_{out} function is the same as 3-input majority function shown in (3) [4].

$$C_{out} = \text{Majority}(A,B,C) = AB + AC + BC \quad (3)$$

This type of majority gate is made of input CNCAPs and a CNFET-based inverter. Figure 3 illustrates a 3-input majority-not gate designed by this method.

$$\begin{aligned} \text{Sum} &= A \oplus B \oplus C \\ &= ABC + \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + A.\overline{B}.\overline{C} = \\ &ABC + (\overline{AB}.\overline{AC}.\overline{BC}).(A+B+C) \\ &= ABC + \overline{C_{out}}.C_{out} + \overline{C_{out}}\ (A+B+C) = \\ &ABC + \overline{C_{out}}\ (AB+AC+BC) + \overline{C_{out}}\ (A+B+C) \\ &= \text{Majority}(A,B,C,\overline{C_{out}},\overline{C_{out}}) \end{aligned} \quad (4)$$

The construction of the proposed design has two stages. $\overline{C_{out}}$ is implemented by means of majority-not function in the first stage and in the second stage a five-input majority-not function is used for implementing $\overline{\text{Sum}}$. Figure 4 illustrates the proposed design. Figure 4(a) exhibits the basic scheme of the design and the circuit is shown in Fig. 4(b). The majority structure is implemented by three input capacitors. These three input capacitors prepare an input voltage that is applied for driving n-CNFET. Through superposition of input capacitors, increase in input voltages is scaled at point x. These capacitors are also connected to $\overline{C_{out}}$ with a capacitor. If "C_1" is the capacitance of each input capacitors, then $2 \times C_2$ is the

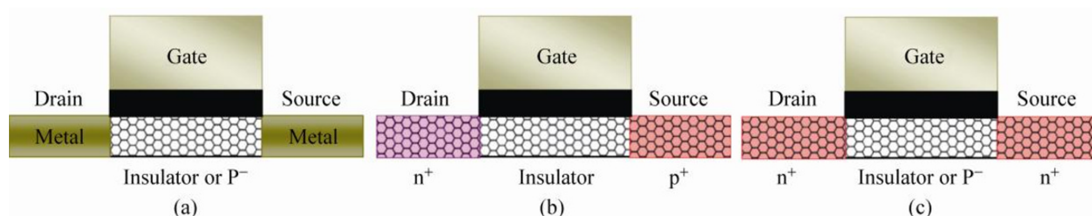


FIG. 2. Different types of the CNFET device. (a) SB-CNFET (b) T-CNFET (c) MOSFET-like CNFET.

capacitance of the capacitor between $\overline{C_{out}}$ and transistor M_2. Thus the capacitance of the capacitor between three input

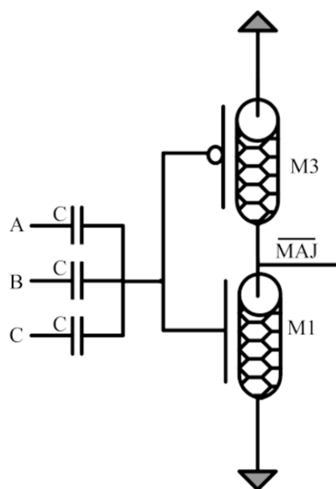
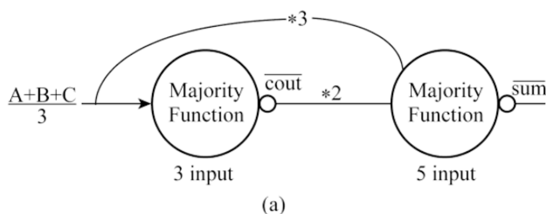


FIG. 3. 3-input Minority circuit.



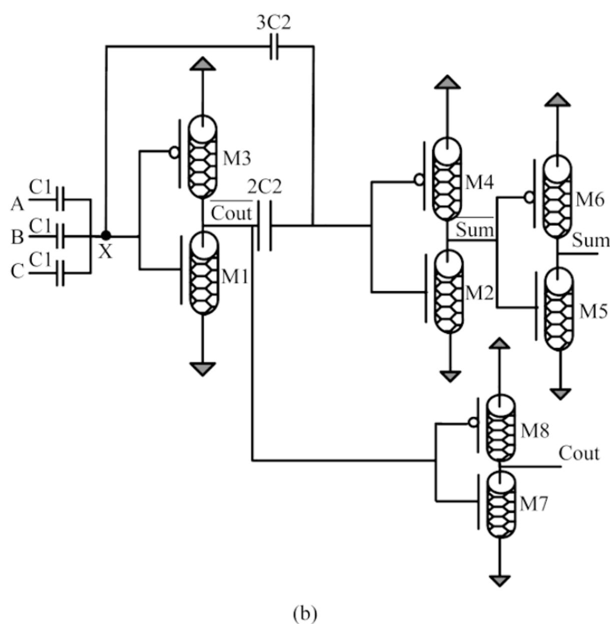


FIG. 4. Proposed design (a) Basic scheme (b) At the transistor level.

capacitors and transistor M2 must be 3×C2.

If more than two inputs becomes high then the M_1 transistor will become ON and in this case the $\overline{C_{out}}$ will fall to "0". Therefore, Cout will be "1". Otherwise, M_1 and M_3 will be OFF and ON respectively and Cout will fall to "0".

The next majority-not gate, which is composed of M_2 and M_4 transistors, has two input capacitors $2\times C_2$ and $3\times C_2$. $2\times C_2$ is driven by $\overline{C_{out}}$ and the input signals drive $3\times C_2$. When all of the inputs are "0", the $\overline{C_{out}}$ will be "1". In this case, the 5-input majority-not gate has three low inputs and two high inputs. Therefore, the $\overline{Sum}$ signal is "1" and Sum is "0". In the case of Sin="1" (for instance "100" input pattern), the majority-not gate has two inputs in the "0" state and three inputs in the "1" state. Hence the Sum signal will be high. When Sin="2" (for instance "110" input pattern) and the input pattern is "111", the Sum signal becomes "0" and "1", respectively.

To implement the capacitors of the proposed circuit, high density CNCAPs [10] are used. Using a $3\times C_2$ capacitor instead of three C_2 capacitors improves the performance of the circuit. Besides, it makes a significant decrease in the circuit area and number of interconnect wires in comparison with CNT-FA-1 and CNT-FA-2. The proposed design utilizes only 5 capacitors and 8 transistors.

Simulation Results Analysis and Comparison

The Synopsys HSPICE circuit simulator has been used to simulate the Full Adders. For simulating CMOS circuits, 32nm CMOS technology has been used. In addition, for CNFET-based circuits, compact SPICE model, including nonidealities proposed in [20-22], has been used for simulations. This standard model has been designed for unipolar, MOSFET-like CNFET devices, in which each transistor may have one or more CNTs. This model also considers Schottky Barrier Effects, Parasitics, including CNT, Source/Drain, and Gate resistances and capacitances, and CNT Charge Screening Effects. The parameters of the CNFET model and their values, with brief descriptions, are shown in Table 1. All of the simulations have been done at room temperature at 0.5 V and 0.65 V supply voltages. The operating frequencies are 250 MHz and 500 MHz. These designs are optimized in terms of PDP (Power Delay Product) [23] at 0.65 V and 250 MHz frequency with 2.1 fF load capacitance. All the possible input transitions are checked and the delay parameter has been measured for each transition. The maximum delay has been chosen as the delay of the circuit. The power consumption parameter has been measured as the average power consumption during a long period of time. Finally, the PDP is calculated for making a

trade-off between speed and power consumption and general performance comparison.

Table 1. CNFET Model Parameters

Parameter	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT channel	100 nm
L_{ss}	The length of doped CNT source-side extension region	32 nm
L_{dd}	The length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

The simulation results of CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-1, CNT-FA-2 and the proposed design in different situations are shown in Table 1. At 0.5v supply voltage, the proposed design is approximately 85.76%, 88.97%, 79.64%, 80.14%, 73.06%, 36.64% and 68.52% faster than CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-1 and CNT-FA-2. The PDP of the proposed design is 79.47%, 82.45%, 67.4%, 70.46%, 60.55%, 52.3% and 46.5% better than CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-2 and CNT-FA-1 respectively. It is 68%, 78.8%, 66.21%, 64.72%, 54.11%, 40.43% and 8.2% faster than CCMOS, Bridge-CMOS, Hybrid1, Hybrid2, TG, CNT-FA-2 and CNT-FA-1 at 0.65 V supply voltage.

The proposed design has the best PDP and delay in comparison with other cells in Table 2 at all supply voltages. Figure 5 shows PDP diagrams in the considered conditions. It can be inferred from the charts that at 250 MHz and 500 MHz frequencies the PDP of the proposed design is less than that of the previous designs. This is due to the shorter critical path of the proposed circuit, which leads to shorter propagation delay and lower number of utilized devices and circuit internal nodes resulting in less capacitance and lower average power consumption.

Figure 6 shows the waveforms of the proposed design at 0.5 V supply voltage. This design performs very well at low supply voltages and high frequencies and has full swing

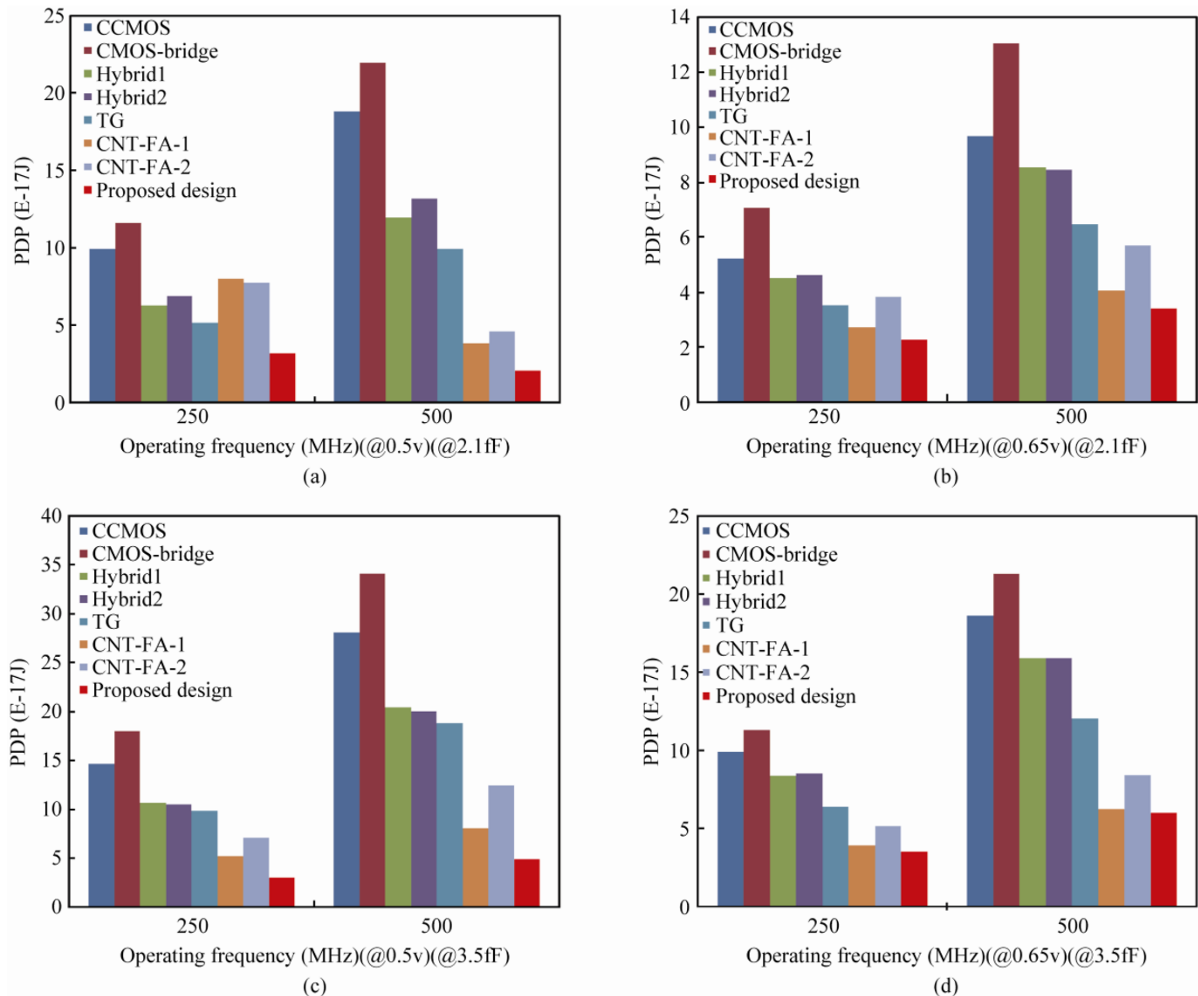


FIG. 5. PDP of the designs at different test conditions.

Table 2. Simulation results for the full adders in 0.5 V and 0.65 V supply voltage

Design	Delay (*10^{-12} Sec)	Power (10^{-7} W)	PDP (10^{-17} J)
		0.5V	
CNT-FA-1	101.37	3.7553	3.8067
CNT-FA-2	204.05	2.2528	4.5969
CCMOS	451.07	2.1982	9.9155
CMOS-Bridge	582.43	1.9915	11.599
Hybrid1	315.57	1.9788	6.2445
Hybrid2	323.47	2.1300	6.8902
TG	238.44	2.1641	5.1602
Proposed Design	64.228	3.1688	2.0353
		0.65V	
CNT-FA-1	45.044	6.0951	2.7455
CNT-FA-2	69.408	5.5519	3.8534
CCMOS	129.40	4.0516	5.2429
CMOS-Bridge	195.05	3.6280	7.0767
Hybrid1	122.38	3.7031	4.5317
Hybrid2	117.20	3.9735	4.6336
TG	90.097	3.9022	3.5157
Proposed Design	41.342	5.4946	2.2716

outputs.

An important attribute of the circuits which should be taken into account is their immunity to the ambient temperature variations [24]. As a result, the circuits have been simulated in a vast range of temperatures, from 0℃ up to 70℃, to evaluate their sensitivity to temperature noises. The results of this experiment, at 0.65 V supply voltage, 250 MHz and with 2.1 fF load capacitance, are plotted in Fig. 7. It can be inferred from Fig. 7 that the proposed design has acceptable functionality and performance in a vast range of temperatures and is superior in terms of PDP, in comparison with the other circuits at all temperatures.

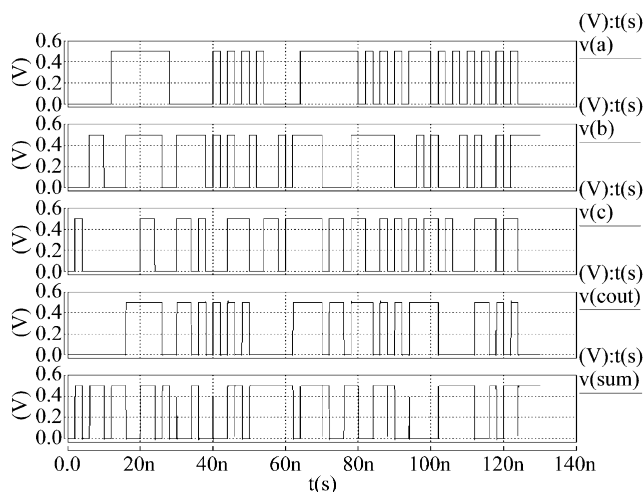


FIG. 6. Input and Output Waveforms of the Proposed Design (@ 250 MHz and 0.5V and with 2.1fF load).

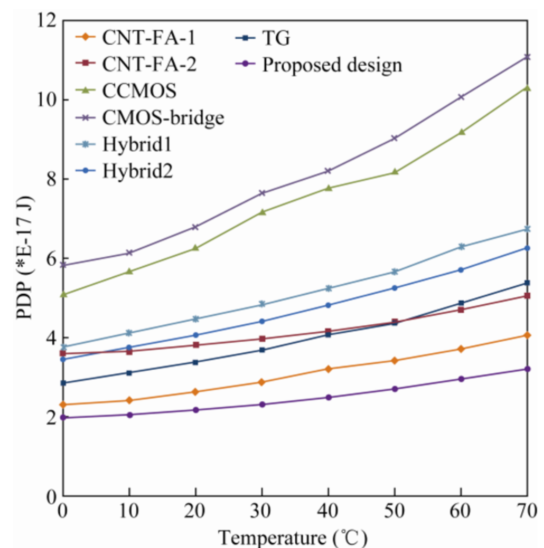


FIG. 7. PDP of the Designs versus Temperature Variations.

Conclusion

This paper has proposed a novel high-speed and low-voltage CNFET-based Full Adder circuit based on Minority function for nanotechnology. This design has rail-to-rail output signals and works properly at low voltages. In order to evaluate its performance some conventional and state-of-the-art 32nm

CMOS and CNFET-based Full Adder designs are simulated. The simulation results indicate that significant improvements in terms of speed and energy efficiency are achievable in different test conditions by utilizing the proposed design.

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