



Cite as  
Nano-Micro Lett.  
(2023) 15:22

## Graphene Bridge Heterostructure Devices for Negative Differential Transconductance Circuit Applications

Received: 21 October 2022  
Accepted: 11 December 2022  
© The Author(s) 2022

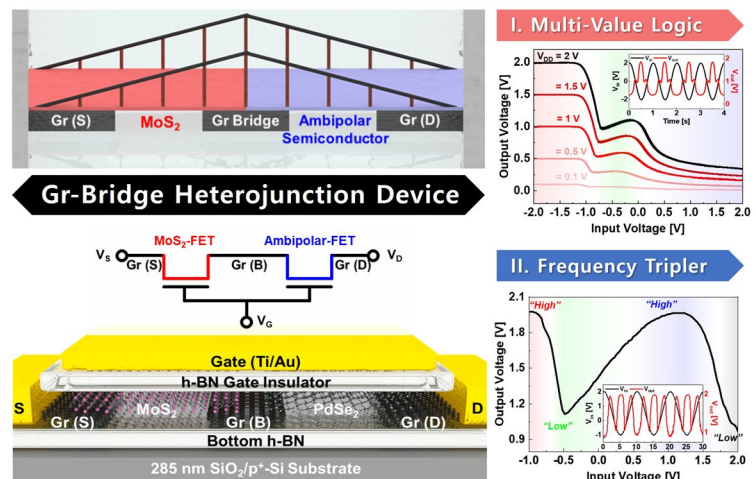
Minjong Lee<sup>1,2</sup>, Tae Wook Kim<sup>3</sup>, Chang Yong Park<sup>1</sup>, Kimoon Lee<sup>4</sup>, Takashi Taniguchi<sup>5</sup>, Kenji Watanabe<sup>5</sup>, Min-gu Kim<sup>1,6</sup> ✉, Do Kyung Hwang<sup>3,7</sup> ✉, Young Tack Lee<sup>1,8</sup> ✉

### HIGHLIGHTS

- Graphene (Gr)-bridge heterostructure, consisting of a laterally series-connected (cascade) ambipolar/Gr/*n*-type 2D van der Waals channel materials for ambipolar semiconductor-based high-end application devices was developed.
- Non-classical transfer characteristics (humped curve) in FET operation and negative differential transconductances were observed.
- Gr-bridge heterostructure device with PdSe<sub>2</sub> (narrow bandgap) allows multi-value logic operation while WSe<sub>2</sub> (wide bandgap) enables frequency tripler circuit operation.

**ABSTRACT** Two-dimensional van der Waals (2D vdW) material-based heterostructure devices have been widely studied for high-end electronic applications owing to their heterojunction properties. In this study, we demonstrate graphene (Gr)-bridge heterostructure devices consisting of laterally series-connected ambipolar semiconductor/Gr-bridge/*n*-type molybdenum disulfide as a channel material for field-effect transistors (FET). Unlike conventional FET operation, our Gr-bridge devices exhibit non-classical transfer characteristics (humped transfer curve), thus possessing a negative differential transconductance. These phenomena are interpreted as the operating behavior in two series-connected FETs, and they result from the gate-tunable contact capacity of the Gr-bridge layer.

Multi-value logic inverters and frequency tripler circuits are successfully demonstrated using ambipolar semiconductors with narrow- and



Minjong Lee, Tae Wook Kim, and Chang Yong Park contributed equally to this work.

✉ Min-gu Kim, mgk@inha.ac.kr; Do Kyung Hwang, dkhwang@kist.re.kr; Young Tack Lee, ytle@inha.ac.kr

<sup>1</sup> Department of Electrical and Computer Engineering, Inha University, Incheon 22212, Republic of Korea

<sup>2</sup> Department of Materials Science and Engineering, The University of Texas at Dallas, Richardson, TX 75080, USA

<sup>3</sup> Center for Opto-Electronic Materials and Devices, Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology (KIST), Seoul 02792, Republic of Korea

<sup>4</sup> Department of Physics, Kunsan National University, Gunsan 54150, Republic of Korea

<sup>5</sup> Advanced Materials Laboratory, National Institute for Materials Science, Tsukuba 305-0044, Japan

<sup>6</sup> Department of Information and Communication Engineering, Inha University, Incheon 22212, Republic of Korea

<sup>7</sup> Division of Nanoscience and Technology, KIST School, University of Science and Technology (UST), Seoul 02792, Republic of Korea

<sup>8</sup> Department of Electronic Engineering, Inha University, Incheon 22212, Republic of Korea

Published online: 29 December 2022



SHANGHAI JIAO TONG UNIVERSITY PRESS

wide-bandgap materials as more advanced circuit applications based on non-classical transfer characteristics. Thus, we believe that our innovative and straightforward device structure engineering will be a promising technique for future multi-functional circuit applications of 2D nanoelectronics.

**KEYWORDS** Graphene bridge; Heterostructure device; Non-classical transfer characteristics; Multi-value logic inverter; Frequency tripler

## 1 Introduction

Two-dimensional van der Waals (2D vdW) nanomaterials have provided intriguing opportunities for various applications in nanoelectronics. For example, graphene (Gr) is a versatile material owing to its excellent carrier mobility and compatibility with various applications; however, the absence of a bandgap limits its use as a semiconductor channel beyond silicon-based electronics [1, 2]. Thus, it can be considered as a conductor material in future electronic devices, and several research groups have used exfoliated Gr as source (S), drain (D), and gate (G) electrodes to achieve all-2D material-based field-effect transistor (FET) applications [3–6]. The Gr S/D electrodes can effectively overcome the Schottky barrier, generally observed between 2D vdW semiconductors and metal contacts [7–10], owing to its gate-dependent Fermi level ( $E_F$ ) modulation [4, 11]. Because of this advantage, Gr electrodes are widely used in 2D vdW materials-based advanced electronic devices, thereby providing an innovative device structure and excellent device performance.

The 2D vdW semiconductors, such as transition metal dichalcogenides (TMDs) and 2D Xenos, have emerged because of their unique electrical properties since the discovery of Gr. Among these, tungsten diselenide ( $WSe_2$ ) and molybdenum ditelluride ( $MoTe_2$ ) possess strong gate-dependent characteristics; essentially, they exhibit ambipolar properties in FET applications [12, 13]. The tunable bandgap of  $WSe_2$  and  $MoTe_2$  is investigated as 1.22 (bulk) to 1.64 eV (monolayer) [14, 15] and 0.9 (bulk) to 1.1 eV (monolayer) [16, 17], respectively. In contrast, black phosphorus (BP) and palladium diselenide ( $PdSe_2$ ), which have narrower bandgaps, exhibit stronger ambipolar properties than  $WSe_2$  and  $MoTe_2$  active channels; therefore, they allow the realization of high-performance device applications. The tunable bandgap of BP and  $PdSe_2$  is reported as 0.3 (bulk) to 1.0 eV (monolayer) [18–20] and near-zero (bulk) to 1.3 eV (monolayer) [21–25], respectively.

These 2D vdW ambipolar semiconductors are expected to open new horizons for future nanoelectronics by developing new functionalized device applications, such as frequency doublers [26–30], reconfigurable homojunction diodes [31–34], and security circuits [35]. In advanced studies on 2D vdW semiconductors, heterostructure devices constructed using various 2D vdW materials as lego-like building blocks have been explored by numerous research groups to fabricate creative device architectures and investigate their unique junction properties [36–39]. A representative assembled device is a vertically stacked heterojunction diode consisting of two 2D vdW semiconductors for photodiodes [40–43], light-emitting diodes [44, 45], Esaki diodes [46–48], and extraordinary applications [49, 50].

In this study, a laterally series-connected ambipolar semiconductor/Gr/*n*-type molybdenum disulfide ( $MoS_2$ ) cascade channel device, called a Gr-bridge heterostructure, was studied beyond heterostructure junction device applications. Each active channel part exhibits distinct transport characteristics, such as ambipolar ( $PdSe_2$  or  $WSe_2$ ), mostly metallic (Gr-bridge), and unipolar ( $MoS_2$ ) properties. However, the series-connected cascade channel combines the transport characteristics of each part, thereby obeying the largest resistance among the channel materials, i.e., the total resistance of the Gr-bridged cascade channel. The Gr-bridge reduces the potential barrier height between the ambipolar semiconductor and *n*-type  $MoS_2$  junction region owing to its metallic and gapless energy band properties. Using this approach, the Gr-bridge allows the realization of unique switching devices and advanced application methods. We successfully demonstrated a multi-value logic inverter circuit and a frequency tripler for advanced electronic applications. Thus, we believe that the Gr-bridge heterojunction structure will open the gate for future electronics by designing device architectures and blending electrical properties toward high-end applications.

## 2 Experimental Section

### 2.1 Device Fabrication

The 285 nm SiO<sub>2</sub>/p<sup>+</sup>-Si substrate was ultrasonically cleaned in acetone, methyl alcohol, and isopropyl alcohol for 15 min each. To construct the Gr-bridge structure, polydimethylsiloxane (PDMS) stamps were used to exfoliate and transfer 2D vdW nanomaterials onto the substrate through the direct imprinting method. Next, a lift-off process was employed to form the top-gate electrode and the extended S/B/D pad electrodes. E-beam lithography and evaporation were, respectively, used for patterning and depositing metal electrodes at the 3D Convergence Center of Inha University.

### 2.2 Electrical Characterization

All transfer, output, and VTC characteristics were measured using a semiconductor parameter analyzer (4156B, Agilent) in a dark probe station at room temperature (300 K). To demonstrate the dynamic performance of the WGM-FET, sinusoidal and ramp waveform signals were generated from a function generator (AFG31022, Tektronix).

## 3 Results and Discussion

### 3.1 2D Ambipolar Semiconductor and Gr-Bridge Heterostructure Device

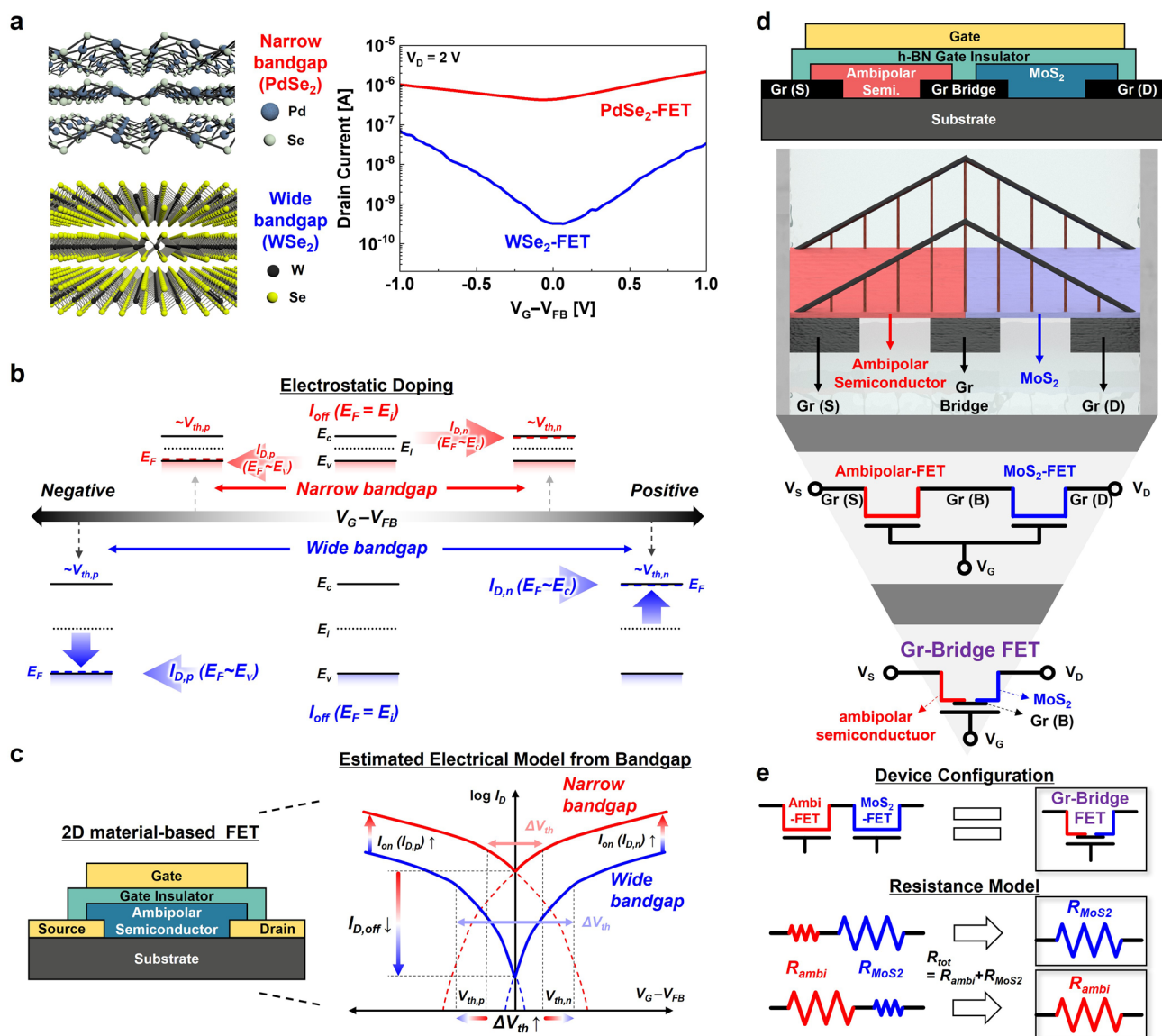
Figure 1a shows the transfer characteristics of PdSe<sub>2</sub> (narrow bandgap, ~0.01 eV) and WSe<sub>2</sub> (wide bandgap, ~1.3 eV) channel-based conventional FET devices [15, 24]. The hexagonal boron nitride (h-BN) sandwich structure and Gr S/D electrodes were adopted to investigate their fundamental ambipolar transfer characteristics ( $I_D$ - $V_G$ ) (see Fig. S1 for the cross-sectional device schematics and optical microscopy (OM) images of the two ambipolar-FET devices). The WSe<sub>2</sub>-FET exhibits both lower drain ON ( $I_{D,p}$  and  $I_{D,n}$ ) and OFF  $I_D$  ( $I_{D,off}$ ) current levels; however, the ON/OFF  $I_D$  ratio ( $I_{ON}/I_{OFF}$ ) is higher than that of the PdSe<sub>2</sub>-FET. The narrow-bandgap materials typically have good electron and hole carrier mobilities;

therefore, they bring a higher ON  $I_D$  value in FET devices but poor OFF  $I_D$  in general. These distinct transfer characteristics are due to their energy bandgap properties, as shown in Fig. 1b.

In 2D vdW ambipolar semiconductors, the gate voltage ( $V_G$ ) can electrostatically control the carrier concentration in the active channel of FET devices, namely the electrostatic doping effect [51]. A positive  $V_G$  over the threshold voltage of the  $n$ -type region ( $V_{th,n}$ ) causes  $E_F$  to reach the conduction-band edge ( $E_c$ ), whereas a negative  $V_G$  near the  $V_{th}$  of the  $p$ -type region ( $V_{th,p}$ ) enables  $E_F$  to reach the valence-band edge ( $E_v$ ) of ambipolar semiconductor channel materials [24, 52, 53]. Consequently, a wider bandgap will result in a larger valley-like transfer characteristic curve because it needs a stronger  $V_G$  (gate field) to modulate the  $E_F$  from the intrinsic Fermi level ( $E_i$ ) to  $E_c$  for the  $n$ -type transition (or the  $E_F$  from  $E_i$  to  $E_v$  for  $p$ -type transition) with a higher  $I_{ON}/I_{OFF}$  ratio.  $E_G$  values of the ambipolar channel materials can be easily estimated by using the  $V_{th}$  difference ( $\Delta V_{th} = V_{th,n} - V_{th,p}$ ) and the average subthreshold slopes [ $SS_{avg} = (SS_n + SS_p)/2$ ] of the  $n$ -type and  $p$ -type regions by Eq. (1), where  $q$  is the electron charge and  $SS_{60}$  is the ideal SS value of 60 mV dec<sup>-1</sup> [24, 35, 52, 53].

$$E_g = \frac{q\Delta V_{th}}{SS_{avg}/SS_{60}} \quad (1)$$

Figure 1c shows the schematic of a typical top-gate transistor device and the expected valley-like transfer characteristic model of ambipolar FETs. The narrow bandgap of the active channel implies that even a small change in  $V_G$  leads to a large number of carriers in the active channel with  $V_{th,n}$  and  $V_{th,p}$  near the transition point (center of the valley-like transfer curve), thereby resulting in a high  $I_{ON}$ , high  $I_{OFF}$ , and low  $I_{ON}/I_{OFF}$  ratio. Although a narrow-bandgap ambipolar semiconductor typically exhibits high-performance FET behavior, the inevitably high  $I_{OFF}$  renders it difficult to use for digital logic circuit applications with better switching characteristics, as compared to wide-bandgap ambipolar semiconductors [35]. Based on the ambipolar properties of PdSe<sub>2</sub> (narrow bandgap) and WSe<sub>2</sub> (wide bandgap) active channel materials, Gr-bridge heterostructure devices have been studied to achieve advanced electronic applications, such as multi-value logic inverters and frequency tripler circuits.



**Fig. 1** **a** Atomic crystal structures and  $I_D$ - $V_G$  transfer characteristic curves of the ambipolar PdSe<sub>2</sub>- and WSe<sub>2</sub>-FETs. **b** Schematic of the relationship between  $E_g$ ,  $V_{th}$ , and  $I_D$  in ambipolar semiconductors. **c** Valley-like estimated electrical transfer model of 2D ambipolar semiconductor-based FETs according to the different energy bandgap properties (narrow and wide bandgap). **d** Conceptual device schematics and suggested electronic component symbol of the Gr-bridge heterostructure device (Gr-bridge FET). **e** Device configuration and resistance-in-series models of Gr-bridge FET

Such devices were formed as a platform of sequentially connected Gr-S, ambipolar semiconductors, Gr-bridge layers, MoS<sub>2</sub>, and Gr-D, as shown in Fig. 1d. The Gr bridge layer allows for the inherent characteristics of each 2D vdW semiconductor because it can provide tunable contact properties to both 2D vdW active channels according to its gate-dependent Fermi level modulation [4, 11]. Essentially, the Gr-bridge FET can be regarded as a series connection of

the ambipolar-FET and MoS<sub>2</sub>-FET, with the same electrical characteristics. Figure 1e shows the simple resistance-in-series model of Gr-bridge FET. The total resistance ( $R_{tot}$ ) depends on the sum of the resistance in each FET part owing to the series connection properties; therefore,  $R_{tot}$  will follow the higher resistance of the two active channels during the device operation. Based on these operating properties, the connected ambipolar and MoS<sub>2</sub> active channel devices in



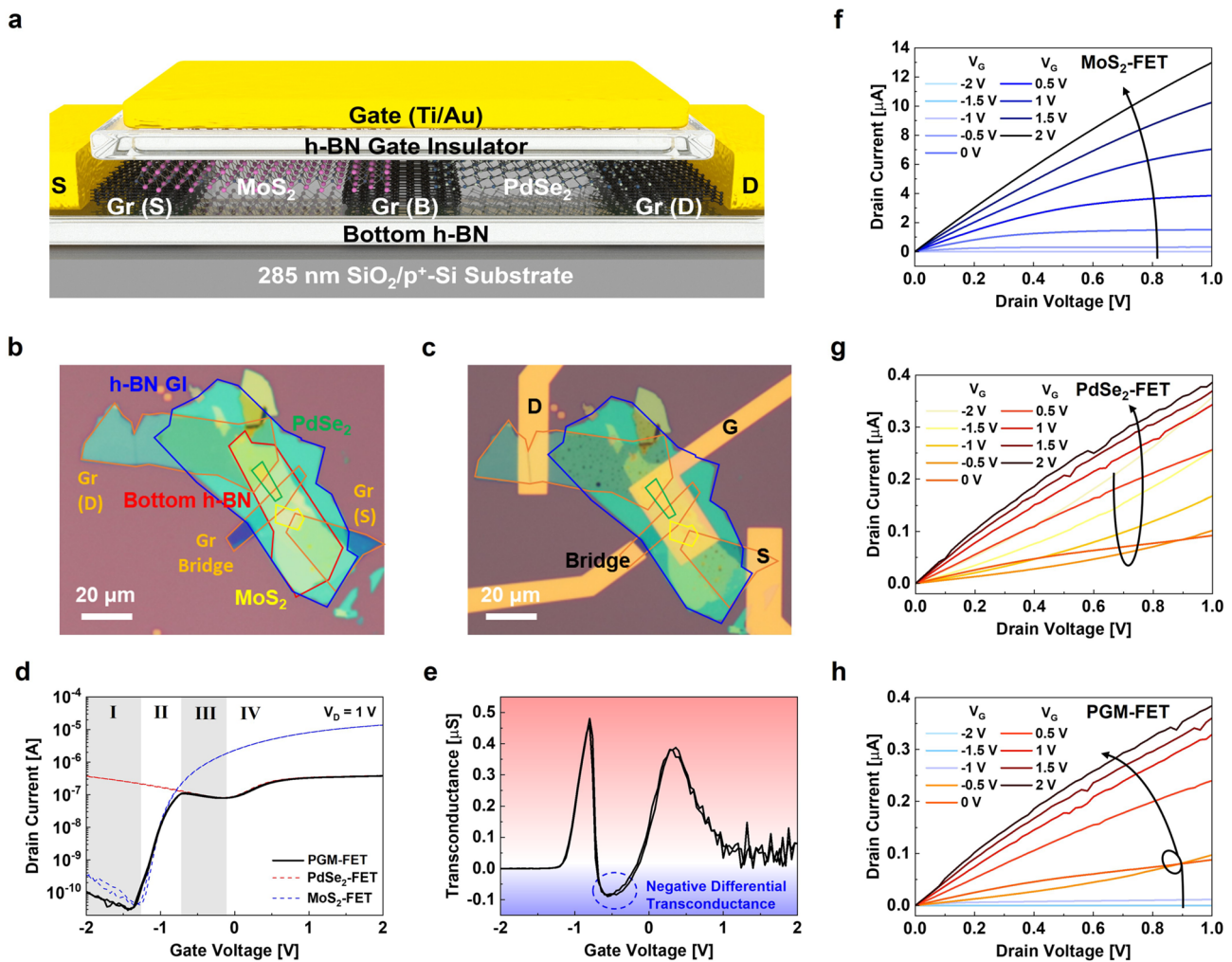
series will exhibit synthetic transfer characteristic curves as a breakthrough for high-end device applications.

### 3.2 PdSe<sub>2</sub>-Gr-MoS<sub>2</sub> Heterostructure FET

The first Gr-bridge-based high-end device consists of ambipolar PdSe<sub>2</sub> (narrow bandgap) and *n*-type MoS<sub>2</sub> active channel materials for multi-value logic applications, as shown in Fig. 2a. Figure 2b, c shows the OM images before and after metal patterning for the extended S/D and common gate (G) electrodes. For sample preparation, the bottom h-BN, Gr S/D, MoS<sub>2</sub>-Gr-PdSe<sub>2</sub> heterostructure, and h-BN gate

insulator were sequentially exfoliated and transferred onto a 285 nm-thick silicon dioxide (SiO<sub>2</sub>)/*p*<sup>+</sup>-silicon (Si) substrate. Subsequently, Ti/Au (5 /50 nm) electrodes were patterned and deposited using a combination of e-beam lithography and e-beam evaporation systems. The detailed step-by-step fabrication flow and thickness information for each 2D vdW material are depicted in Fig. S2 and S3, respectively.

Figure 2d shows the *I*<sub>D</sub>-*V*<sub>G</sub> transfer curves of the MoS<sub>2</sub>-FET (blue dashed line), PdSe<sub>2</sub>-FET (red dashed line), and PdSe<sub>2</sub>-Gr-MoS<sub>2</sub> heterostructure devices (solid black line) at a drain voltage (*V*<sub>D</sub>) of 1 V. We named the Gr-bridge device (PdSe<sub>2</sub>-Gr-MoS<sub>2</sub> FET) “PGM-FET.” Because the h-BN sandwich structure was adopted to



**Fig. 2** a Cross-sectional 3D device schematic of the PdSe<sub>2</sub>-Gr-MoS<sub>2</sub> heterostructure FET (PGM-FET) for multi-value logic applications. OM images of the PGM-FET b before and c after the extended metal electrode fabrication. d *I*<sub>D</sub>-*V*<sub>G</sub> transfer characteristic curves of the MoS<sub>2</sub>-FET (blue dashed line), PdSe<sub>2</sub>-FET (red dashed line), and PGM-FET (black solid line) at *V*<sub>D</sub> of 1 V. e Estimated transconductance of the PGM-FET obtained from *I*<sub>D</sub>-*V*<sub>D</sub> output characteristic curves of f MoS<sub>2</sub>-FET, g PdSe<sub>2</sub>-FET, and h PGM-FET. (Color figure online)

provide high-quality interfaces, hysteresis-less ideal transfer properties exist in all FET operations [54–57]. The MoS<sub>2</sub>-FET exhibits strong *n*-type transfer characteristics, and the PdSe<sub>2</sub>-FET shows ambipolar transfer characteristics using the Gr bridge layer as a source. Because the graphene interlayer has a gate-tunable contact capacity, it can act as a “bridge,” thereby reducing the Schottky junction properties between the ambipolar and *n*-type active channels. The detailed Raman spectrum analysis to confirm the clean and non-interactive interface properties of Gr-bridge and TMDC channels are shown in Fig. S4. Owing to the effect of the Gr bridge interconnection, the PGM-FET exhibits a tilde (~) symbol-like humped transfer characteristic curve: it traces the lower *I<sub>D</sub>* of either the PdSe<sub>2</sub> or MoS<sub>2</sub> FETs according to the swept *V<sub>G</sub>* (see the solid black line in Fig. 2d). The *I<sub>D</sub>* of the PGM-FET follows the *I<sub>OFF</sub>* (region I) and subthreshold *I<sub>D</sub>* (region II) of the MoS<sub>2</sub>-FET, while regions III and IV, respectively, denote the case in the transfer *I<sub>D,p</sub>* and *I<sub>D,n</sub>* of PdSe<sub>2</sub>.

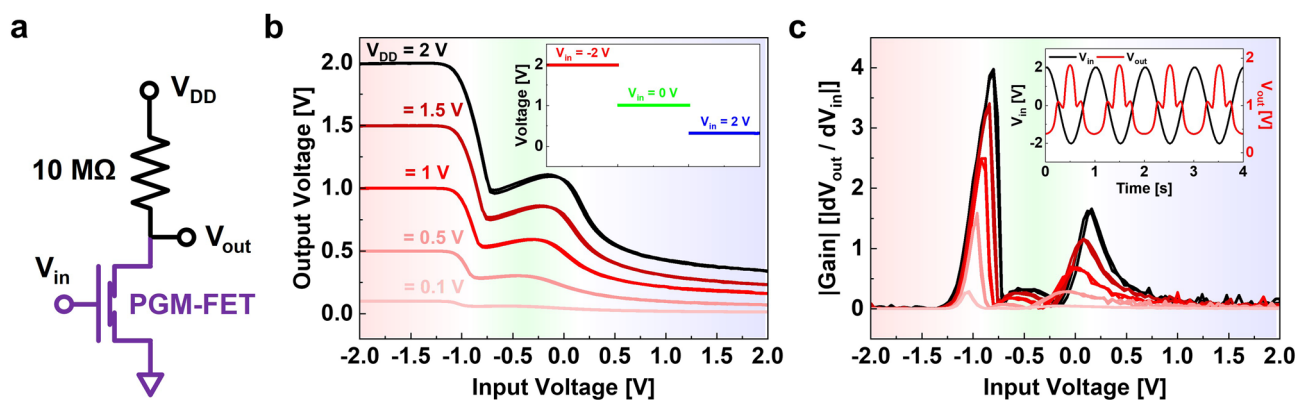
To analyze the detailed transport properties of the PGM-FET, the transconductance ( $g_m = dI_D/dV_G$ ) was calculated, and a negative  $g_m$  was observed in region III (humped curve), as shown in Fig. 2e. Figure 2f–h shows the output characteristic (*I<sub>D</sub>*–*V<sub>D</sub>*) curves of the MoS<sub>2</sub>-FET, PdSe<sub>2</sub>-FET, and PGM-FET obtained from *V<sub>G</sub>* ranging from –2 to 2 V in steps of 0.5 V. The Gr bridge provides tunable ohmic contact properties; therefore, the output curves of the MoS<sub>2</sub> and PdSe<sub>2</sub> active channels exhibit typical *n*-type and ambipolar transport properties, respectively. Moreover, the PGM-FET exhibits the composite output characteristics of the

MoS<sub>2</sub>-FET (*V<sub>G</sub>* range of –2 to –1 V) and PdSe<sub>2</sub>-FET (*V<sub>G</sub>* range of –0.5 to 2 V).

### 3.3 PGM-FET-Based Multi-value Logic Circuit Applications

Based on the non-classical humped *I<sub>D</sub>*–*V<sub>G</sub>* transfer properties, we extended our PGM-FET study to multi-value logic circuit applications as a first-approach method. An external resistor of 10 MΩ was chosen for the resistive-load inverter circuit near the humped *I<sub>D</sub>* curve, as shown in Fig. 3a. Figure 3b shows the voltage transfer characteristics (VTC) of the PGM-FET-based resistive-load inverter circuit under different supply voltage (*V<sub>DD</sub>*) conditions. The inset shows three distinct levels of ternary inverted output voltage (*V<sub>out</sub>*) responses. Input voltages (*V<sub>in</sub>*) of –2, 0, and 2 V generate *V<sub>out</sub>* of *V<sub>DD</sub>*, *V<sub>DD</sub>*/2, and approximately 0 V, respectively. Figure 3c shows the absolute voltage gain ( $dV_{out}/dV_{in}$ ) of the ternary inverter logic circuit under different *V<sub>DD</sub>* conditions. The voltage gain is approximately 4 (first voltage drop) and approximately 1.6 (second voltage drop) at a *V<sub>DD</sub>* of 2 V. The inset shows the dynamic *V<sub>out</sub>* responses obtained from a sinusoidal waveform of *V<sub>in</sub>*, which can identify the dynamic ternary levels of the demonstrated ternary logic circuit. The peak-to-peak voltage (*V<sub>p-p</sub>*) and periodic time (*T*) were 4 V and 1 s, respectively.

We developed inverted ternary logic for the Gr-bridge structure, which simply employs a narrow-bandgap ambipolar semiconductor (PdSe<sub>2</sub>) and an *n*-type semiconductor

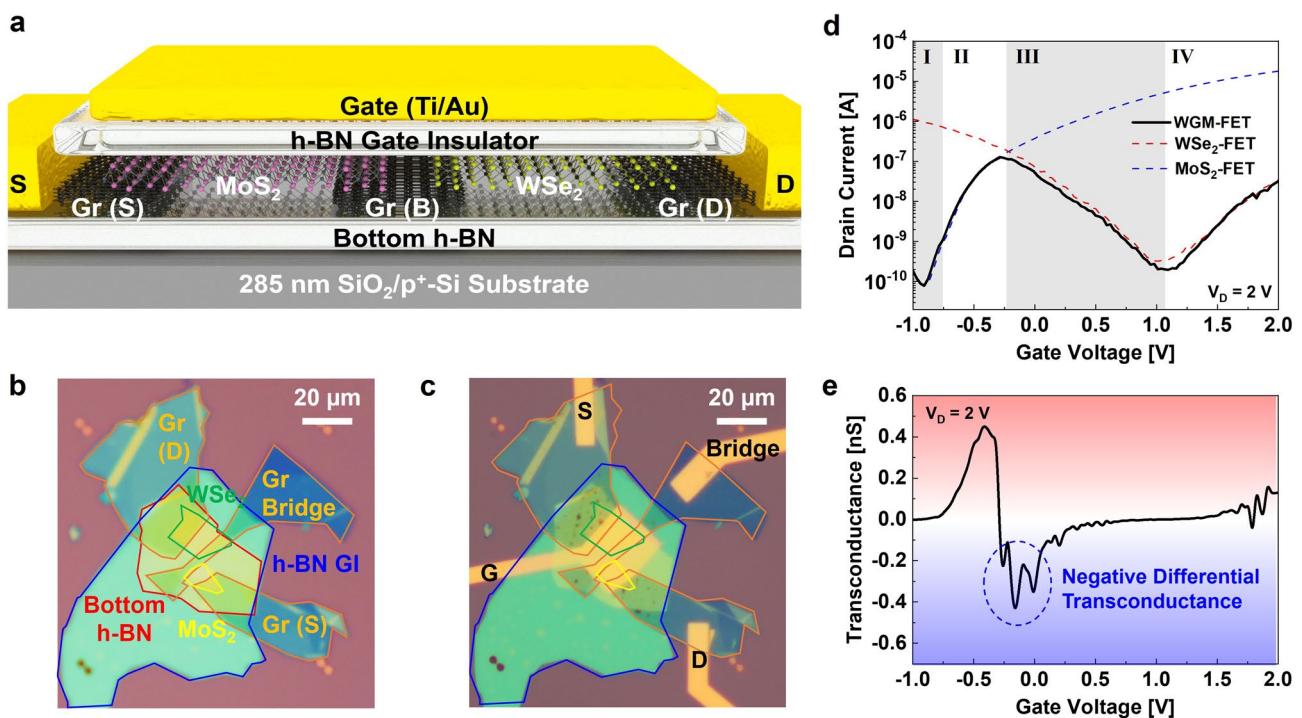


**Fig. 3** **a** Circuit diagram of PGM-FET-based resistive-load inverter for multi-value logic circuit applications. **b** VTC characteristic curves of PGM-FET-based multi-value logic operations for *V<sub>DD</sub>* ranging from 0.1 to 2 V. The inset shows three distinguished output states (ternary logic states). **c** Voltage gain of the demonstrated ternary inverter logic circuit for *V<sub>DD</sub>* ranging from 0.1 to 2 V. The inset shows the dynamic *V<sub>out</sub>* responses (red) from the sinusoidal waveform *V<sub>in</sub>* (black). (Color figure online)

(MoS<sub>2</sub>). Based on the above understanding of the PGM-FET-based ternary logic circuit, we attempted to investigate a direct PdSe<sub>2</sub>-MoS<sub>2</sub> junction FET (PMJ-FET) for a more advanced and practical device model, as shown in Fig. S5. Although the PMJ-FET also exhibits a non-classical humped  $I_D-V_G$  transfer curve and ternary logic circuit operation, the absence of the Gr-bridge interlayer results in rectifying properties at the PdSe<sub>2</sub>/MoS<sub>2</sub> junction [58]. Consequently, the PMJ-FET exhibits asymmetric (having direction) device characteristics and a limitation in dynamic operation, whereas the PGM-FET exhibits symmetric (bidirectional) logic circuit operation properties. Furthermore, reliability problems remain in the PMJ-FET because controlling the optimized junction properties between the two different semiconductor active channels is difficult. As shown in Fig. S4d, the PMJ-FET does not trace the transfer curves of the MoS<sub>2</sub>-FET and PdSe<sub>2</sub>-FET because of the rectifying junction properties of MoS<sub>2</sub>/PdSe<sub>2</sub> [42]. Therefore, adopting the Gr-bridge device structure will provide reliability and convenience for further study of high-end multi-value logic applications.

### 3.4 WSe<sub>2</sub>-Gr-MoS<sub>2</sub> Heterostructure FET Device

As a second approach toward advanced electronic applications, WSe<sub>2</sub>, a wide-bandgap ambipolar active channel, was chosen to realize the Gr-bridge heterostructure device instead of the PdSe<sub>2</sub>-based ternary logic circuit. Figure 4a shows the 3D device schematic of WSe<sub>2</sub>-Gr-MoS<sub>2</sub> FET, named “WGM-FET.” Figure 4b, c shows the OM images before and after patterning of the extended S/D and G electrodes, respectively, through the same device fabrication processes of PGM-FET. The detailed process flow and thickness information for each layer are shown in Figs. S6 and S7, respectively. Figure 4d shows the  $I_D-V_G$  transfer curves of the MoS<sub>2</sub>-FET (blue dashed line), WSe<sub>2</sub>-FET (red dashed line), and WGM-FET (solid black line) at  $V_D$  of 2 V. In this case, the transfer curve of WGM-FET follows that of the MoS<sub>2</sub>-FET in regions I and II and that of WSe<sub>2</sub>-FET in regions III and IV. However, unlike the case of PGM-FET, the wider bandgap of the WSe<sub>2</sub> channel allows a low  $I_{OFF}$  level of WGM-FET (wider region III); therefore, the transfer characteristic curves resemble an uppercase letter



**Fig. 4** **a** Cross-sectional 3D device schematic of the WSe<sub>2</sub>-Gr-MoS<sub>2</sub> heterostructure FET (WGM-FET) for frequency tripler circuit applications. OM images of the WGM-FET **b** before and **c** after the extended metal electrode fabrication. **d**  $I_D-V_G$  transfer characteristic curves of the MoS<sub>2</sub>-FET (blue dashed line), WSe<sub>2</sub>-FET (red dashed line), and WGM-FET (black solid line). **e** Estimated transconductances of the WGM-FET obtained from **d**. (Color figure online)

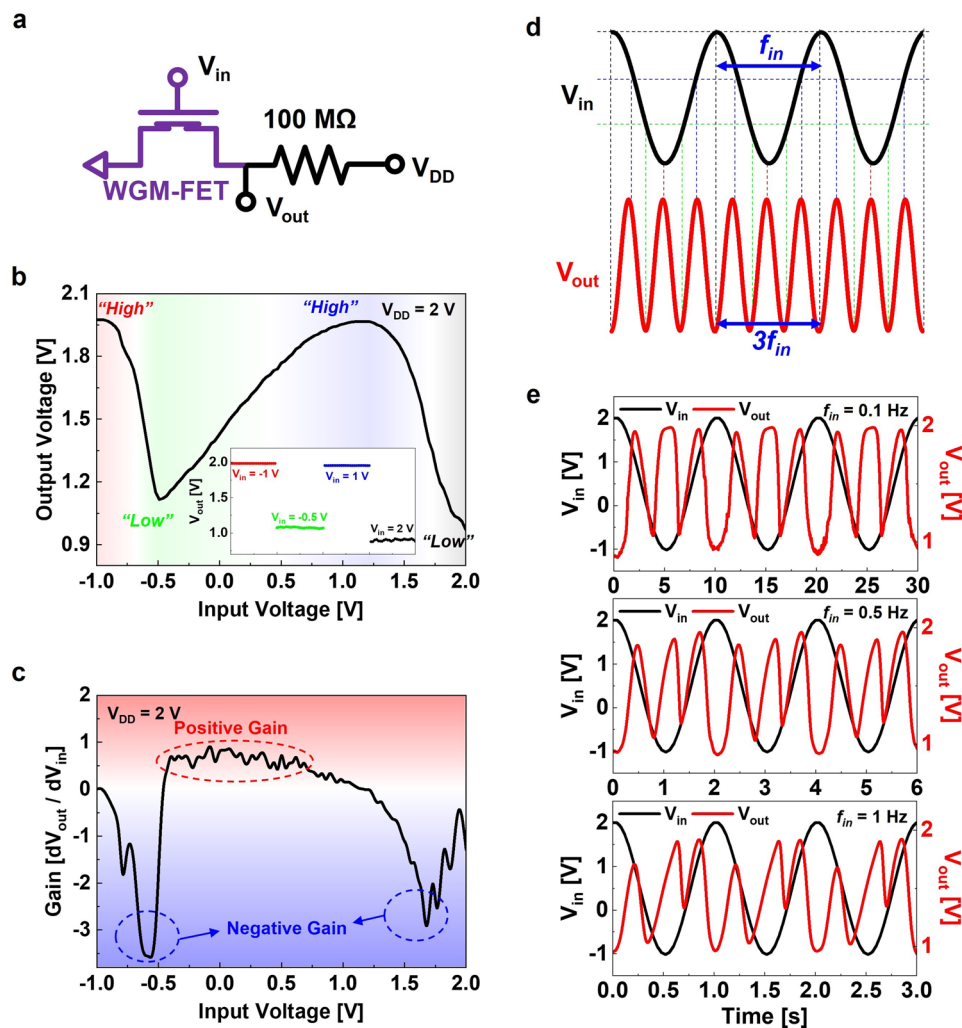
“N”. Figure 4e shows the  $g_m$ – $V_G$  curve of the WGM-FET; a negative  $g_m$  was observed in operation region III owing to the  $p$ -type transition properties of the  $\text{WSe}_2$  active channel.

### 3.5 WGM-FET-Based Frequency Tripler Circuit Applications

These non-classical transfer characteristics of the WGM-FET bring unique VTC characteristics of an upside-down letter “N”-like curve in inverter logic circuit applications, as shown in Fig. 5a. To achieve a resistive-load inverter circuit,

an external resistor of 100 M $\Omega$  was connected to the WGM-FET. Figure 5b shows the VTC curve, and the four transition states were observed as sequentially “High”, “Low”, “High”, and “Low” output states according to the voltage sweep of  $V_{in}$  at  $V_{DD}$  of 2 V. The inset shows the four distinguished logic states at  $V_{in}$  of  $-1$ ,  $-0.5$ ,  $1$ , and  $2$  V. Figure 5c shows the voltage gain of our demonstrated inverter circuit, which has both negative and positive values.

The  $V_{in}$  sweep from “Low ( $-1$  V)” to “High ( $2$  V)” should produce sequential output states of “High–Low–High–Low” and the backward  $V_{in}$  sweep from “High” to “Low” generated the reversed output states of



**Fig. 5** **a** Circuit diagram of the WGM-FET-based resistive-load inverter circuit applications. **b** Upside-down letter “N”-like VTC curve of WGM-FET-based frequency tripler circuit operations at  $V_{DD}$  of 2 V. The inset shows four distinguished output states, that is, sequentially repeated “High” and “Low” states. **c** Voltage gain of the demonstrated WGM-FET-based frequency tripler circuit. **d** Expected frequency response of frequency tripler (three cycles of  $V_{out}$ ) converted from a single cycle of  $V_{in}$ . **e** Real-time  $V_{out}$  responses (red) of the frequency tripler circuit for 0.1, 0.5, and 1 Hz input sinusoidal waveform  $V_{in}$  (black). (Color figure online)



“Low–High–Low–High.” That is, a double sweep of  $V_{in}$  of “Low–High–Low,” similar to a single waveform, will produce the “High–Low–High–Low–High–Low–High” sequential output states. The repeatable “High” and “Low” output logic states enable an advanced frequency response application with respect to the sinusoidal waveform of  $V_{in}$ , as shown in Fig. 5d. As a result, a single cycle of sinusoidal waveform  $V_{in}$  should produce three cycles of the waveform  $V_{out}$ . This circuit application method can be regarded as a “frequency tripler,” which can generate the output frequency ( $f_{out}$ ) to triple the value from the input frequency ( $f_{in}$ ). Finally, for the first time, we successfully demonstrated a frequency tripler application with a single Gr-bridge heterostructure FET consisting of a wide-bandgap ambipolar semiconductor. Figure 5e shows the real-time  $V_{out}$  responses for the 0.1, 0.5, and 1 Hz sinusoidal waveforms of  $V_{in}$  (see Fig. S8 for the real-time  $V_{out}$  response for the 1 Hz ramp waveform  $V_{in}$ ). The  $V_{out}$  responses were analyzed using fast Fourier transform (FFT), as shown in Fig. S9. Our frequency response application should be economical to generate triple frequency toward low-power (frequency) and low-cost, more effective than the conventional frequency multiplier circuit for future advanced electronics.

## 4 Conclusions

In this study, Gr-bridge FETs consisting of laterally series-connected ambipolar semiconductor/Gr-bridge/ $n$ -type  $\text{MoS}_2$  cascade channels were studied for high-end switching device applications based on their non-classical negative differential transconductance characteristics. The Gr-bridge layer could eliminate the Schottky junction properties between two semiconductor channels; therefore, the Gr-bridge FETs showed synthetic transfer characteristics, perfectly tracing the lower  $I_D$  of each channel material based on the simple resistance-in-series model, unlike the heterojunction devices without the Gr-bridge layer. Moreover, we successfully implemented two types of advanced electronic applications based on the bandgap properties of  $\text{PdSe}_2$  (narrow-bandgap) and  $\text{WSe}_2$  (wide-bandgap) ambipolar semiconductors for a multi-value logic inverter (PGM-FET) and frequency tripler (WGM-FET) circuits, respectively. Thus, we believe that the results of our

Gr-bridge heterostructure devices and multi-functional circuit applications will provide reliability and convenience to open up a breakthrough toward future advanced electronics.

**Acknowledgements** Y. T. L. acknowledges the financial support from the National Research Foundation of Korea (NRF) (No. NRF-2021R1C1C1005235). D. K. H. acknowledges the financial support from the Korea Institute of Science and Technology (KIST) Institution Program (No. 2E31532).

**Funding** Open access funding provided by Shanghai Jiao Tong University.

**Open Access** This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article’s Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article’s Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit <http://creativecommons.org/licenses/by/4.0/>.

**Supplementary Information** The online version contains supplementary material available at <https://doi.org/10.1007/s40820-022-01001-5>.

## References

1. A. Das, S. Pisana, B. Chakraborty, S. Piscanec, S.K. Saha et al., Monitoring dopants by raman scattering in an electrochemically top-gated graphene transistor. *Nat. Nanotechnol.* **3**, 210–215 (2008). <https://doi.org/10.1038/nnano.2008.67>
2. F. Schwierz, Graphene transistors. *Nat. Nanotechnol.* **5**, 487–496 (2010). <https://doi.org/10.1038/nnano.2010.89>
3. J. Tang, Q. Wang, Z. Wei, C. Shen, X. Lu et al., Vertical integration of 2D building blocks for all-2D electronics. *Adv. Electron. Mater.* **6**(12), 2000550 (2020). <https://doi.org/10.1002/aelm.202000550>
4. K. Choi, Y.T. Lee, J.S. Kim, S.-W. Min, Y. Cho et al., Non-lithographic fabrication of all-2D  $\alpha$ - $\text{MoTe}_2$  dual gate transistors. *Adv. Funct. Mater.* **26**(18), 3146–3153 (2016). <https://doi.org/10.1002/adfm.201505346>
5. G.H. Lee, X. Cui, Y.D. Kim, G. Arefe, X. Zhang et al., Highly stable, dual-gated  $\text{MoS}_2$  transistors encapsulated by hexagonal boron nitride with gate-controllable contact, resistance, and threshold voltage. *ACS Nano* **9**(7), 7019–7026 (2015). <https://doi.org/10.1021/acs.nano.5b01341>

6. M. Lee, C.Y. Park, D.K. Hwang, M. Kim, Y.T. Kee, Longitudinal and latitudinal split-gate field-effect transistors for NAND and NOR logic circuit applications. *npj 2D Mater. Appl.* **6**, 45 (2022). <https://doi.org/10.1038/s41699-022-00320-w>
7. S. Das, H.Y. Chen, A.V. Penumatcha, J. Appenzeller, High performance multilayer MoS<sub>2</sub> transistors with scandium contacts. *Nano Lett.* **13**(1), 100–105 (2013). <https://doi.org/10.1021/nl303583v>
8. Y. Xu, C. Cheng, S. Du, J. Yang, B. Yu et al., Contacts between two- and three-dimensional materials ohmic, schottky and p-n heterojunctions. *ACS Nano* **10**(5), 4895–4919 (2016). <https://doi.org/10.1021/acs.nano.6b01842>
9. A. Allain, J. Kang, K. Banerjee, A. Kis, Electrical contacts to two-dimensional semiconductors. *Nat. Mater.* **14**, 1195–1205 (2015). <https://doi.org/10.1038/nmat4452>
10. K. Sotthewes, R. van Bremen, E. Dollekamp, T. Boulogne, K. Nowakowski et al., Universal Fermi-level pinning in transition-metal dichalcogenides. *J. Phys. Chem. C* **123**(9), 5411–5420 (2019). <https://doi.org/10.1021/acs.jpcc.8b10971>
11. Y.T. Lee, K. Choi, H.S. Lee, S.W. Min, P.-J. Jeon et al., Graphene versus ohmic metal as source-drain electrode for MoS<sub>2</sub> nanosheet transistor channel. *Small* **10**(12), 2356–2361 (2014). <https://doi.org/10.1002/sml.201303908>
12. S. Nakaharai, M. Yamamoto, K. Ueno, K. Tsukagoshi, Carrier polarity control in  $\alpha$ -MoTe<sub>2</sub> schottky junctions based on weak Fermi-level pinning. *ACS Appl. Mater. Interfaces* **8**(23), 14732–14739 (2016). <https://doi.org/10.1021/acsami.6b02036>
13. S. Das, J. Appenzeller, WSe<sub>2</sub> field effect transistors with enhanced ambipolar characteristics. *Appl. Phys. Lett.* **103**, 103501 (2013). <https://doi.org/10.1063/1.4820408>
14. S. Sharma, C. Ambrosch-Draxl, M.A. Khan, P. Blaha, S. Auluck, Optical properties and band structure of 2H-WSe<sub>2</sub>. *Phys. Rev. B* **60**(12), 8610–8615 (1999). <https://doi.org/10.1103/PhysRevB.60.8610>
15. G.H. Yousefi, Optical properties of mixed transition metal dichalcogenide crystals. *Mater. Lett.* **9**(1), 0167–577x (1989). [https://doi.org/10.1016/0167-577X\(89\)90128-6](https://doi.org/10.1016/0167-577X(89)90128-6)
16. I.G. Lezama, A. Arora, A. Ubaldini, C. Barreateau, E. Gianini et al., Indirect-to-direct band gap crossover in few-layer MoTe<sub>2</sub>. *Nano Lett.* **15**(4), 2336–2342 (2015). <https://doi.org/10.1021/nl5045007>
17. C. Ruppert, O.B. Aslan, T.F. Heinz, Optical properties and band gap of single- and few-layer MoTe<sub>2</sub> crystals. *Nano Lett.* **14**(11), 6231–6236 (2014). <https://doi.org/10.1021/nl502557g>
18. L. Li, Y. Yu, G.J. Ye, Q. Ge, X. Ou et al., Black phosphorus field-effect transistors. *Nat. Nanotechnol.* **9**, 372–377 (2014). <https://doi.org/10.1038/nnano.2014.35>
19. Y. Du, H. Liu, Y. Deng, P.D. Ye, Device perspective for black phosphorus field-effect transistors: contact resistance, ambipolar behavior, and scaling. *ACS Nano* **8**(10), 10035–10042 (2014). <https://doi.org/10.1021/nn502553m>
20. H. Liu, A.T. Neal, Z. Zhu, Z. Luo, X. Xu et al., An unexplored 2D semiconductor with a high hole mobility. *ACS Nano* **8**(4), 4033–4041 (2014). <https://doi.org/10.1021/nn501226z>
21. L.-S. Lu, G.-H. Chen, H.-Y. Cheng, C.-P. Chuu, K.-C. Lu et al., Layer-dependent and in-plane anisotropic properties of low-temperature synthesized few-layer PdSe<sub>2</sub> single crystals. *ACS Nano* **14**(4), 4963–4972 (2020). <https://doi.org/10.1021/acsnano.0c01139>
22. C. Xie, S. Jiang, Y. Gao, M. Hong, S. Pan et al., Giant thickness-tunable bandgap and robust air stability of 2D palladium diselenide. *Small* **16**(19), 2000754 (2020). <https://doi.org/10.1002/sml.202000754>
23. A.D. Oyedele, S. Yang, L. Liang, A.A. Puretzy, K. Wang et al., PdSe<sub>2</sub>: pentagonal two-dimensional layers with high air stability for electronics. *J. Am. Chem. Soc.* **139**(40), 14090–14097 (2017). <https://doi.org/10.1021/jacs.7b04865>
24. M. Lee, C.Y. Park, S. Sim, K. Lee, Y.T. Lee, Homogeneous palladium diselenide pn-junction diodes for reconfigurable circuit applications. *Adv. Electron. Mater.* **8**(10), 2101282 (2022). <https://doi.org/10.1002/aelm.202101282>
25. Y. Wang, J. Pang, Q. Cheng, L. Han, Y. Li et al., Applications of 2D-layered palladium diselenide and its van der Waals heterostructures in electronics and optoelectronics. *Nano-Micro Lett.* **13**, 143 (2021). <https://doi.org/10.1007/s40820-021-00660-0>
26. T.W. Kim, H.S. Ra, J. Ahn, J. Jang, T. Taniguchi et al., Frequency doubler and universal logic gate based on two-dimensional transition metal dichalcogenide transistors with low power consumption. *ACS Appl. Mater. Interfaces* **13**(6), 7470–7475 (2021). <https://doi.org/10.1021/acsami.0c21222>
27. W. Fu, L. Feng, D. Mayer, G. Panaitov, D. Kireev et al., Electrolyte-gated graphene ambipolar frequency multipliers for biochemical sensing. *Nano Lett.* **16**(4), 2295–2300 (2016). <https://doi.org/10.1021/acs.nanolett.5b04729>
28. P. Golani, H. Yun, S. Ghosh, J. Wen, K.A. Mkhoyan et al., Ambipolar transport in van der Waals black arsenic field effect transistors. *Nanotechnology* **31**, 405203 (2020). <https://doi.org/10.1088/1361-6528/ab9d40>
29. C. Pan, Y. Fu, J. Wang, J. Zeng, G. Su et al., Analog circuit applications based on ambipolar graphene/MoTe<sub>2</sub> vertical transistors. *Adv. Electron. Mater.* **4**(3), 1700662 (2018). <https://doi.org/10.1002/aelm.201700662>
30. S. Yu, Y. Cho, J.Y. Lim, H. Kwon, Y. Jeong et al., Advanced multifunctional field effect devices using common gate for both 2D transition-metal dichalcogenide and InGaZnO channels. *Adv. Electron. Mater.* **5**(12), 1900730 (2019). <https://doi.org/10.1002/aelm.201900730>
31. G. Wu, X. Wang, Y. Chen, S. Wu, B. Wu et al., MoTe<sub>2</sub> p–n homojunctions defined by ferroelectric polarization. *Adv. Mater.* **32**(16), 1907937 (2020). <https://doi.org/10.1002/adma.201907937>
32. M. Buscema, D.J. Groenendijk, G.A. Steele, H.S.J. van der Zant, A. Castellanos-Gomez, Photovoltaic effect in few-layer black phosphorus pn junctions defined by local electrostatic gating. *Nat. Commun.* **5**, 4651 (2014). <https://doi.org/10.1038/ncomms5651>
33. A. Pospischil, M.M. Furchi, T. Mueller, Solar-energy conversion and light emission in an atomic monolayer p–n diode.

- Nat. Nanotechnol. **9**, 257–261 (2014). <https://doi.org/10.1038/nnano.2014.14>
34. Y.-Q. Bie, G. Grosso, M. Heuck, M.M. Furchi, Y. Cao et al., A MoTe<sub>2</sub>-based light-emitting diode and photodetector for silicon photonic integrated circuits. Nat. Nanotechnol. **12**, 1124–1129 (2017). <https://doi.org/10.1038/nnano.2017.209>
35. P. Wu, D. Reis, X.S. Hu, J. Appenzeller, Two-dimensional transistors with reconfigurable polarities for secure circuits. Nat. Electron. **4**, 45–53 (2021). <https://doi.org/10.1038/s41928-020-00511-7>
36. A.K. Geim, I.V. Grigorieva, van der Waals heterostructures. Nature **499**, 419–425 (2013). <https://doi.org/10.1038/nature12385>
37. J.D. Yao, G.W. Yang, All-2D architectures toward advanced electronic and optoelectronic devices. Nano Today **36**, 101026 (2021). <https://doi.org/10.1016/j.nantod.2020.101026>
38. S. Kim, G. Myeong, W. Shin, H. Lim, B. Kim et al., Thickness-controlled black phosphorus tunnel field-effect transistor for low-power switches. Nat. Nanotechnol. **15**, 203–206 (2020). <https://doi.org/10.1038/s41565-019-0623-7>
39. S. Park, H.J. Lee, W. Choi, H.-J. Jin, H. Cho et al., Quaternary NAND logic and complementary ternary inverter with p-MoTe<sub>2</sub>/n-MoS<sub>2</sub> heterostack channel transistors. Adv. Funct. Mater. **32**(13), 2108737 (2022). <https://doi.org/10.1002/adfm.202108737>
40. D. Wu, J. Guo, J. Du, C. Xia, L. Zeng et al., Highly polarization-sensitive, broadband, self-powered photodetector based on graphene/PdSe<sub>2</sub>/germanium heterojunction. ACS Nano **13**(9), 9907–9917 (2019). <https://doi.org/10.1021/acsnano.9b03994>
41. A.M. Afzal, G. Dastgeer, M.Z. Iqbal, P. Gautam, M.M. Faisal, High-performance p-BP/n-PdSe<sub>2</sub> near-infrared photodiodes with a fast and gate-tunable photoresponse. ACS Appl. Mater. Interfaces **12**(17), 19625–19634 (2020). <https://doi.org/10.1021/acsmi.9b22898>
42. M. Long, Y. Wang, P. Wang, X. Zhou, H. Xia et al., Palladium diselenide long-wavelength infrared photodetector with high sensitivity and stability. ACS Nano **13**(2), 2511–2519 (2019). <https://doi.org/10.1021/acsnano.8b09476>
43. J. Pang, Y. Wang, X. Yang, L. Zhang, Y. Li et al., A wafer-scale two-dimensional platinum monosulfide ultrathin film via metal sulfurization for high performance photoelectronics. Mater. Adv. **3**, 1497–1505 (2022). <https://doi.org/10.1039/D1MA00757B>
44. M. Paur, A.J.M. Mendoza, R. Bratschitsch, K. Watanabe, T. Taniguchi et al., Electroluminescence from multi-particle exciton complexes in transition metal dichalcogenide semiconductors. Nat. Commun. **10**, 1709 (2019). <https://doi.org/10.1038/s41467-019-09781-y>
45. P. Li, K. Yuan, D.Y. Lin, X. Xu, Y. Wang et al., A mixed-dimensional light-emitting diode based on a p-MoS<sub>2</sub> nanosheet and an n-CdSe nanowire. Nanoscale **9**, 18175 (2017). <https://doi.org/10.1039/C7NR05706G>
46. T. Roy, M. Tosun, X. Cao, H. Fang, D.H. Lien et al., Dual-gated MoS<sub>2</sub>/WSe<sub>2</sub> van der Waals tunnel diodes and transistors. ACS Nano **9**(2), 2071–2079 (2015). <https://doi.org/10.1021/nn507278b>
47. J. Shim, S. Oh, D.H. Kang, S.H. Jo, M.H. Ali et al., Phosphorene/rhenium disulfide heterojunction-based negative differential resistance device for multi-valued logic. Nat. Commun. **7**, 13413 (2016). <https://doi.org/10.1038/ncomms13413>
48. N. Oliva, J. Backman, L. Capua, M. Cavalieri, M. Luisier et al., WSe<sub>2</sub>/SnSe<sub>2</sub> vdW heterojunction tunnel FET with sub-thermionic characteristic and MOSFET co-integrated on same WSe<sub>2</sub> flake. npj 2D Mater. Appl. **4**, 5 (2020). <https://doi.org/10.1038/s41699-020-0142-2>
49. W. Wang, Z. Li, M. Li, L. Fang, F. Chen et al., High-transconductance, highly elastic, durable and recyclable all-polymer electrochemical transistors with 3D micro-engineered interfaces. Nano-Micro Lett. **14**, 184 (2022). <https://doi.org/10.1007/s40820-022-00930-5>
50. L. Zhou, K. Wang, H. Sun, S. Zhao, X. Chen et al., Novel graphene biosensor based on the functionalization of multifunctional nano-bovine serum albumin for the highly sensitive detection of cancer biomarkers. Nano-Micro Lett. **11**, 20 (2019). <https://doi.org/10.1007/s40820-019-0250-8>
51. W. Hu, Z. Sheng, X. Hou, H. Chen, Z. Zhang et al., Ambipolar 2D semiconductors and emerging device applications. Small Methods **5**(1), 2000837 (2021). <https://doi.org/10.1002/smdt.202000837>
52. H. Tian, B. Deng, M.L. Chin, X. Yan, H. Jiang et al., A dynamically reconfigurable ambipolar black phosphorus memory device. ACS Nano **10**(11), 10428–10435 (2016). <https://doi.org/10.1021/acsnano.6b06293>
53. H. Xu, S. Fathipour, E.W. Kinder, A.C. Seabaugh, S.K. Fullerton-Shirey, Reconfigurable 1ion gating of 2H-MoTe<sub>2</sub> field-effect transistors using poly(ethylene oxide)-CsClO<sub>4</sub> solid polymer electrolyte. ACS Nano **9**(5), 4900–4910 (2015). <https://doi.org/10.1021/nn506521p>
54. C.R. Dean, A.F. Young, I. Meric, C. Lee, L. Wang et al., Boron nitride substrates for high-quality graphene electronics. Nat. Nanotechnol. **5**, 722–726 (2010). <https://doi.org/10.1038/nnano.2010.172>
55. E. Wu, Y. Xie, J. Zhang, H. Zhang, X. Hu et al., Dynamically controllable polarity modulation of MoTe<sub>2</sub> field-effect transistors through ultraviolet light and electrostatic activation. Sci. Adv. **5**(5), eaav3430 (2019). <https://doi.org/10.1126/sciadv.aav3430>
56. G.H. Lee, Y.J. Yu, X. Cui, N. Petrone, C.H. Lee et al., Flexible and transparent MoS<sub>2</sub> field-effect transistors on hexagonal boron nitride-graphene heterostructures. ACS Nano **7**(9), 7931–7936 (2013). <https://doi.org/10.1021/nn402954e>
57. M.Y. Chan, K. Komatsu, S.L. Li, Y. Xu, P. Darmawan et al., Suppression of thermally activated carrier transport in atomically thin MoS<sub>2</sub> on crystalline hexagonal boron nitride substrates. Nanoscale **5**, 9572–9576 (2013). <https://doi.org/10.1039/c3nr03220e>
58. M. Huang, S. Li, Z. Zhang, X. Xiong, X. Li et al., Multifunctional high-performance van der Waals heterostructures. Nat. Nanotechnol. **12**, 1148–1154 (2017). <https://doi.org/10.1038/nnano.2017.208>

