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REVIEW

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Chalcogenide Ovonic Threshold Switching Selector

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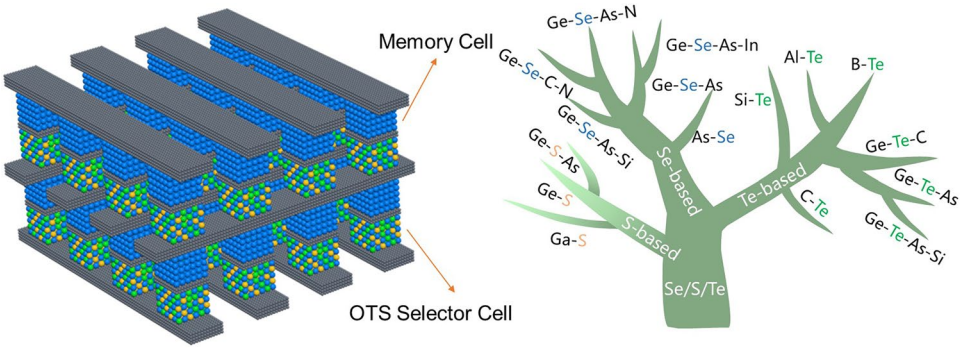
HIGHLIGHTS

- The development history and key milestones of ovonic threshold switch (OTS) materials were comprehensively summarized. Combined with the latest advancements of OTS research, the mainstream OTS material systems were systematically introduced.
- A thorough overview of the prevailing viewpoints regarding the OTS switching mechanisms was presented.
- Recent progress in OTS devices for applications in 3D memory, self-selecting memory, and neuromorphic computing was summarized.

ABSTRACT Today's explosion of data urgently requires memory technologies capable of storing large volumes of data in shorter time frames, a feat unattainable with Flash or DRAM. Intel Optane, commonly referred to as three-dimensional phase change memory, stands out as one of the most promising candidates. The Optane with cross-point architecture is constructed through layering a storage element and a selector known as the ovonic threshold switch (OTS). The OTS device, which employs chalcogenide film, has thereby gathered increased attention in recent years. In this paper, we begin by providing a brief introduction to the discovery process of the OTS phenomenon. Subsequently, we summarize the key electrical parameters of OTS devices and delve into recent explorations of OTS materials, which are categorized as Se-based, Te-based, and S-based material systems. Furthermore, we discuss various models for the OTS switching mechanism, including field-induced nucleation model, as well as several carrier injection models. Additionally, we review the progress and innovations in OTS mechanism research. Finally, we highlight the successful application of OTS devices in three-dimensional high-density memory and offer insights into their promising performance and extensive prospects in emerging applications, such as self-selecting memory and neuromorphic computing.



KEYWORDS Non-volatile memory; Ovonic threshold switch (OTS); Chalcogenide; Selector

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1 Introduction

The era of big data and AIoT (Artificial Intelligence and Internet of Things) necessitates the novel memory technologies for massive and quick integration of data storage, which is predicted to reach 175 ZB (1 zettabyte = 10^{21} byte) in 2025 [1]. The 3D stackable emerging non-volatile memory has become a key solution to address the challenge. In 3D high-density stacking, as process nodes continue to shrink from hundreds of nanometers to a few nanometers, the spacing between the parallel memory cells in the stack decreases, resulting in an increased load on the metal interconnects (Fig. 1a). "Leakage current" or "sneak current" becomes an unavoidable issue. Leakage current can cause crosstalk between neighboring memory cells, affecting read and write operation, interfering with stored data, reducing storage lifespan, and increasing power consumption [2–4]. To effectively suppress leakage current, it is essential to control all possible leakage paths. The most efficient solution is to directly connect each memory cell to an independent device called "selector," forming the memory array.

The selector is not simply a dielectric layer material or a high-resistance device; it appears to be simple but has several requirements. From a functional perspective, the selector must be an independent device with switch function (Fig. 1b). Considering high integration density, simple two-terminal structures, capable of vertically stacking with the memory cell, would significantly increase the spatial utilization [2]. Additionally, the selector needs to accurately control the selected storage unit when activated, strictly prevent the selection of other storage units, and maximize the suppression of leakage current in these unselected cells. The selector thereby should exhibit low leakage current in the off-state, while providing sufficient high drive current in the on-state. Furthermore, as the most common operation in memory, that is, read/write operation, needs to switch on/off the selector cell, the selector should have high stability and endurance [5]. From the perspective of the memory system, the performance of the selector should be compatible with the operation logic of the peripheral circuitry, necessitating high operational speed (switching speed) to accommodate high-speed read and write operation. Moreover, it is preferable for the selector to have bi-directional select capability to adapt to different operation rules. From a manufacturing process standpoint, the selector should have good compatibility with CMOS technology and not damage the memory cells during fabrication. Therefore, the research on selector is of great importance and has even become one of the core issues in 3D high-density memory.

After decades of effort, many selector candidates have been proposed (Fig. 2), such as traditional PNP junctions [6], mixed ion–electron conductor (MIEC) [7], metal–insulator transition (MIT) [8, 9], ion-diffusion threshold switching [10] as well as ovonic threshold switch (OTS) [11]. Among them, chalcogenide-based OTS selector, which exhibits distinct high drive current, nanosecond speed, low leakage current, and excellent scalability, is the only one that has been successfully used in commercial 3D memory

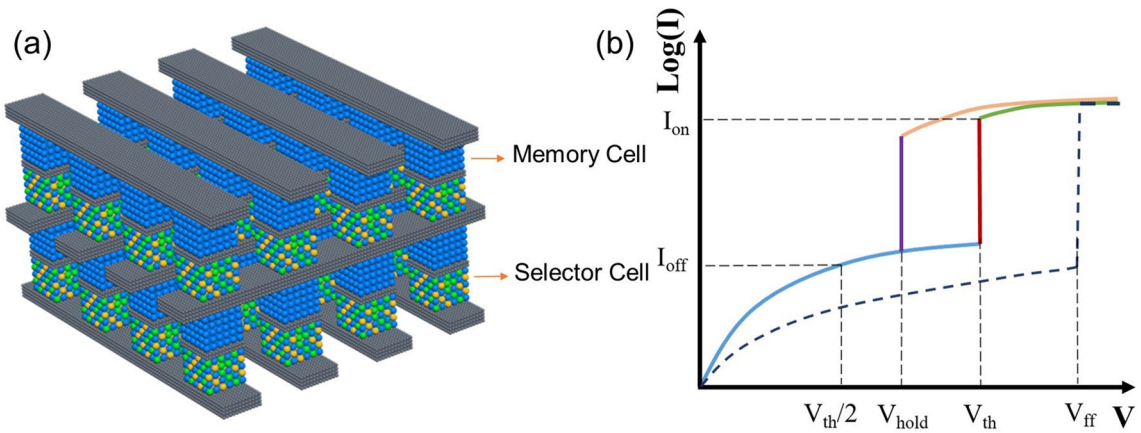

Fig. 1 3D Crosspoint architecture (**a**) and typical current–voltage (*I-V*) curve of the selector cell (**b**). A first fire voltage (V_{ff}) is required to operate the selector cell. Then, a relative low voltage, called threshold voltage (V_{th}), can turn on the cell, which would return to the off-state as the voltage decreases to the hold voltage (V_{hold}). $V_{ff} > V_{th} > V_{hold}$

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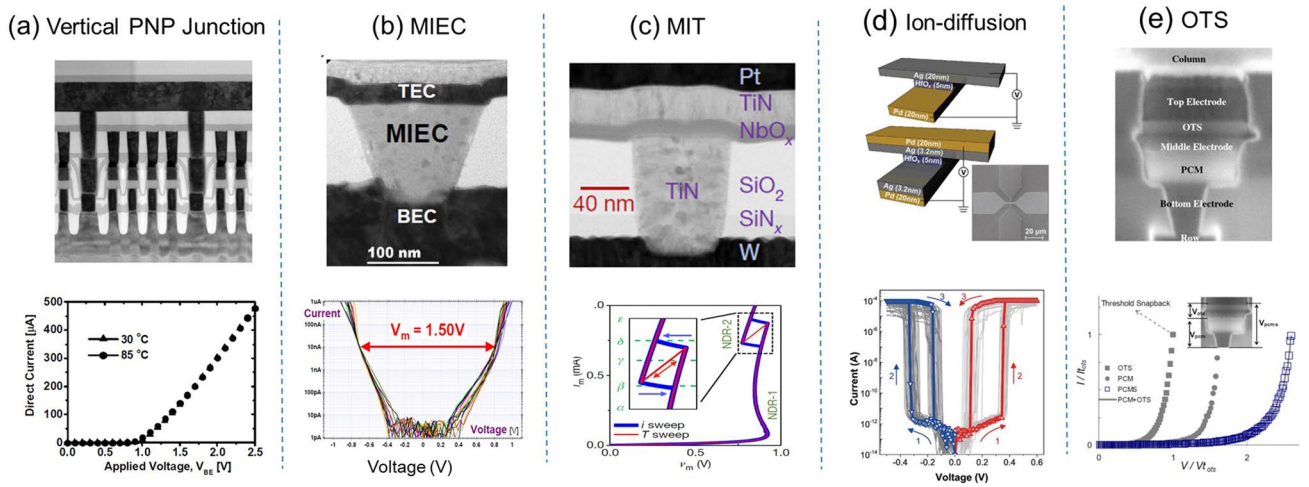

Fig. 2 Various selector candidates. **a** Vertical PNP junctions. Adapted with permission from [6]. Copyright 2009, IEEE. **b** Mixed ion–electron conductor (MIEC). Adapted with permission from [7]. Copyright 2012, IEEE. **c** Metal–insulator transition (MIT). Adapted with permission from [9]. Copyright 2017, Springer Nature. **d** Ion-diffusion threshold switching. Adapted with permission from [10]. Copyright 2017, John Wiley and Sons. **e** Ovonic threshold switching (OTS). Adapted with permission from [11]. Copyright 2009, IEEE

chips, namely Optane by Intel [12]. In this paper, we first briefly introduce the discovery process of the OTS phenomenon. Next, we summarize the key electrical parameters of OTS devices and discuss the recent explorations of OTS materials, which are classified as Se-based, Te-based, and S-based material systems. Furthermore, we address the various theoretical explanations for the OTS switching behavior, listing the diverse perspectives and reviewing the progress and innovations in OTS mechanism research. Finally, we highlight the successful application of OTS devices in three-dimensional high-density memory, and we provide insights into their promising performance and extensive prospects in emerging applications such as self-selecting memory and neuromorphic computing.

2 Discovery of OTS Phenomenon

In 1964, Northover and Pearson from Bell Telephone Laboratories first observed the threshold switching (TS) phenomenon in As–Te–I [13]. This phenomenon refers to a rapid increase in electrical conductivity and a transition to a low-resistance state (on-state) when a specific threshold voltage (V_{th}) is reached under applied external voltage. Dennard also found this phenomenon in As–Te–Se [14]. In 1966, S.R. Ovshinsky applied for a patent [15], in which he reported his findings on reversible switching in memory devices composed of 48 at.% tellurium, 30 at.% arsenic, 12 at.% silicon, and 10 at.% germanium (amorphous $Te_{48}As_{30}Si_{12}Ge_{10}$). Then, in his paper published in 1968 [16], he notes at the end that "an unusual memory effect is observed in materials in which structural changes are facilitated by the removal of cross-linking elements from the above formula—for example, the reduction of arsenic to 5 at.%. After switching from a highly resistive state, structural changes result in the preservation of a conductive state even when the current is totally removed. The material can be reversibly switched back to the highly resistive state by application of a current pulse of either polarity exceeding a threshold value."

From a modern perspective, these descriptions imply three key points. Firstly, chalcogenide devices exhibiting the TS phenomenon can display volatile (returning to the initial low-conductivity state after removing external excitation) or non-volatile (maintaining a high-conductivity state after removing external excitation) electrical behaviors, which are later known as OTS and ovonic memory switch (OMS), respectively. Secondly, the same material system can exhibit memory potential by modifying the composition (As < 5 at.%), establishing a basis for future composition optimization and selector/memory applications. Thirdly, a short and high-amplitude current pulse can be applied to achieve the state transition in OMS devices, which laid the foundation for the future RESET operation in phase change memory (PCM), enabling controllable and reversible phase change operation.

The concept of OTS itself represents a categorization of specific electrical performance in materials rather than a physical definition. Broadly speaking, material systems that exhibit the OTS phenomenon and meet specific criteria can be referred to as OTS materials. The distinction between OTS and OMS (also known as PCM) material systems, as well as the analysis of specific parameters, remains a focal point in chalcogenide research. In 1970, D.L. Nelson from Ovshinsky's company (Energy Conversion Devices) explicitly delineated the electrical characteristic differences between OTS and OMS and successfully fabricated the first storage array with independent OTS and OMS structures, as displayed in Fig. 3, a precursor to the 1S1R (S: selector; R: resistance/memory) structure for today's 3D memory architecture [17]. Although chalcogenide TS devices demonstrated typical switching performance, their goal of replacing Si-based and Ge-based transistors was not successfully achieved in practice at that time. However, non-volatile chalcogenide TS devices, later known as PCM, gradually gained widespread application in the field of optical storage after the discovery of GeTe–Sb_2Te_3 pseudo-binary alloys [18, 19] and subsequent Ag–In–Sb–Te materials [20, 21].

Although both optical and electrical differences between the crystalline and amorphous states of PCM were discovered, the development of electrical storage using PCM progressed slowly due to limitations imposed by the semiconductor fabrication technology at that time [22]. It was not until the early twenty-first century, with the scaling down of integrated circuit process nodes to 180 nm, that PCM gained significant attention again due to its fast switching speed [23, 24], large resistance contrast, and excellent scalability [20]. Since 2001, major storage companies worldwide, including Intel, Samsung, IBM, Micron, and STMicroelectronics, have conducted research on PCM and subsequently introduced their storage product, in which traditional transistors were applied as the selector cell, including MOSFETs, PN diodes and vertical PNP junctions [6]. Although 4 Mb to 8 Gb PCM chips were fabricated [21, 24–27], the fact that the transistor cannot survive without the silicon substrate makes it impossible to achieve multiple-desks stacking for 3D high-density memory. Noticeably, in 2009, Intel and Numonyx proposed a novel scalable and stackable memory [11], built by layering an OMS and an OTS, which was a crucial milestone in the ultimate commercialization of 128 Gb PCM-based 3D Xpoint in 2017. Since then, OTS selectors have emerged as the most promising selector in the new generation of 3D stacked memories, and more and more novel OTS materials were explored.

3 OTS Materials and Device

OTS materials, discovered during the same period as PCM, are primarily composed of chalcogenide. Besides the slight difference in stoichiometry, OTS materials are only found in the amorphous state, whereas crystalline phase are still needed for the PCM [23]. Therefore, a stable amorphous system, which can withstand 400–450 °C annealing for 30 min in the back-end-of-line process [29], is often sought in the

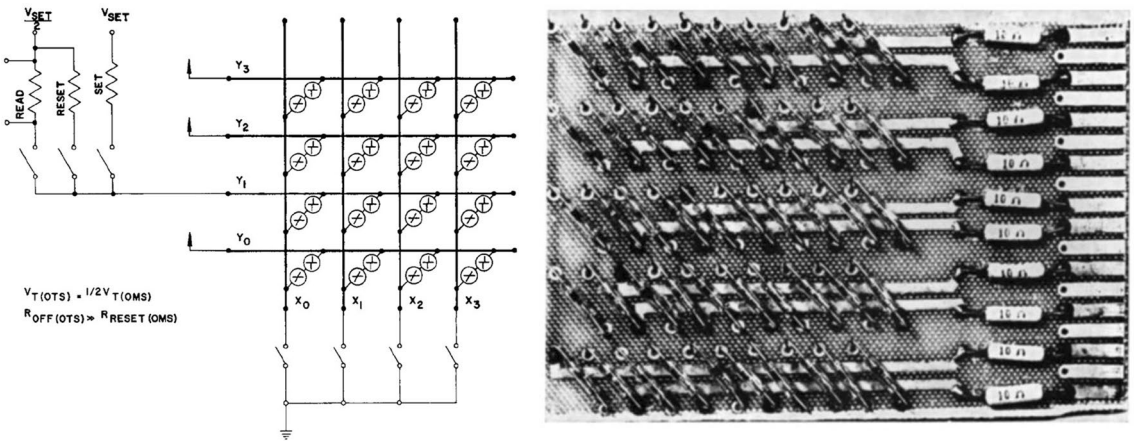

Fig. 3 Schematic diagram and photograph of an OTS + OMS array. Adapted with permission from [17]. Copyright 1970, Elsevier

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design of OTS materials. The OTS devices have a sandwich structure, and exhibit two states: on and off states. As shown in Fig. 1b, a first fire voltage (V_{ff}) is required to operate the selector cell. Then a rather low voltage, called threshold voltage (V_{th}), can turn on the cell (on-state), which could return to the off-state as the voltage decreases to the hold voltage (V_{hold}). Therefore, $V_{ff} > V_{th} > V_{hold}$. Specific electrical parameters of OTS devices are: (1) on-state current (I_{on})/current density (J_{on}), (2) off-state leakage current (I_{off}), (3) on/off ratio or selectivity, (4) endurance, (5) thermal stability, (6) threshold voltage/field (V_{th}/E_{th}), and (7) switching speed (t_{on}/t_{off}). Appropriate control of these electrical parameters can greatly satisfy the application of OTS in storage devices, as well as its application in other fields.

For 3D high-density memory applications, there are several requirements for the OTS device, which exhibit significant correspondences to material properties, as summarized in Table 1. Firstly, in order to successfully drive the connected memory cell, the OTS cell requires a large driving current density, for example, greater than 10 MA cm^{-2} for 3D PCM [28, 29]. This necessitates OTS materials with saturated covalent bond to provide a more robust amorphous network, thus tolerating high passing I_{on} current without abundantly breaking the bonds and recrystallization. Secondly, to achieve > Mb-scale capacity storage, the leakage current (I_{off}) of the OTS device, obtained at $V_{th}/2$, should be suppressed below 10^{-8}A and a selectivity (I_{on}/I_{off}) of at least 10^4 is needed [4, 30]. This requires materials with a big mobility gap and thereby high activity barrier [31, 32]. Thirdly, as the most frequent read operation in practical 3D memory needs to switch on/off the OTS selector, the endurance of the OTS device should be several orders of magnitude higher than the one of the memory unit (typically 10^6 cycles for PCM and resistance random access memory RRAM [20, 33]), that is, exceeding 10^8 cycles for the OTS cell. This necessitates OTS materials with high thermal stability (to avoid crystallization-caused failure) and no phase separation during operation. Fourthly, the amorphous state of OTS device should be able to withstand a temperature of 400–450 °C in the back-end-of-line (BEOL) process since the OTS behavior disappears upon crystallization, in which the insulator and contact metal layers are deposited [29, 34]. This requires the crystallization temperature of the amorphous OTS material to be higher than 400 °C. Fifthly, to be compatible with advanced logic applications (e.g., 3.3 V for *I/O* pin) and also reduce the power consumption, an OTS cell with a low V_{th} are recommended [35]. This implies that the material's mobility gap and trap state density should not be too large. Obviously, this requirement is contrary to that of low I_{off}; therefore, a comprehensive consideration is needed. To achieve high-speed storage, the switching speed of the OTS device should be within 100 ns, faster or comparable with the memory units. This requires the OTS material to be chalcogenides without Ag, Cu, etc., active elements, avoiding atomic diffusion and maintaining an electron-dominated switching process. In addition, the drift of V_{th} (i.e., the change of V_{th} over time after the operation) in OTS materials is also a noteworthy issue; V_{th} drift should be as small as possible. It should be noted that the OTS device structure (such as OTS material layer thickness, multi-layer structure [36]) and operation mode [37] can also affect the overall device performance.

The development of OTS material systems is not confined to a single pathway. Specifically, the research on OTS material compositions generally exhibits a trend from simplicity to complexity. Typically, the development

Table 1 The application of 3D memory requires OTS materials to meet many requirements

Key parameters	Application requirement	Material requirement
On-state current (I_{on})/current density (J_{on})	> 10 MA cm^{-2} for PCM applications	Saturated covalent bond
Off-state leakage current (I_{off})	< 10^{-8} A	Big mobility gap
I_{on}/I_{off} or selectivity	> 10^4 for 1 Mb memory array	Strong bond and big mobility gap
Endurance	> 10^8 cycles	High crystallization temperature and no phase segregation
Thermal stability	400–450 °C annealing for 30 min	> 400 °C crystallization temperature
Threshold voltage (V_{th})	< 3.3 V	Relatively low mobility gap and trap state density
Switching speed (t_{on}/t_{off})	< 100 ns	Inert material to avoid the diffusion

starts with a simple basic material with good performance, which is then analyzed and optimized to address any deficiencies. Through doping and compositional optimization, a multi-component material system is eventually established. The reasons for this development trend are multifaceted [29]. Firstly, in the research and development of OTS switch devices, optimization of specific components is often carried out for engineering considerations or the need for mechanism studies to enhance certain performance indicators. Secondly, the successful application of OTS devices in commercial products is exciting, but the process of commercialization introduces additional considerations such as cost, process compatibility, and environmental impact. These new requirements drive innovation and optimization of OTS materials. Lastly, the optimization and innovation of a material system are often propelled by the advancement of its mechanism research. Different theoretical analyses and explanations of OTS switching mechanisms lead to variations, and the optimization of performance under different theories will employ different compositional optimization methods.

Doping processes and compositional optimization, as typical means of material performance enhancement, are also applicable to OTS devices. It is evident that the introduction of a new element usually affects more than one key parameter, regardless of the initial purpose of its introduction. From a material design perspective, the incorporation of elements such as Ge, As, Si, C, N, and B can improve the material's crystallization temperature, stabilize the amorphous system, or reduce leakage by introducing elements with wider mobility gap. Subsequently, targeted improvements can be made based on the defects in these binary compounds. The participation of these elements, with varying relative concentrations, often nonlinearly affects electrical parameters such as V_{th} and I_{off}. Therefore, the composition of OTS materials is not a simple superposition of fixed doping elements. On the contrary, these elements interact with each other in a multi-component system, and the addition of some elements may even cause the system to lose its OTS characteristics. Although dozens of OTS materials have been explored since 1966, Se, Te, and S chalcogens are essential elements, as summarized in Fig. 4, which are discussed in detail as follows.

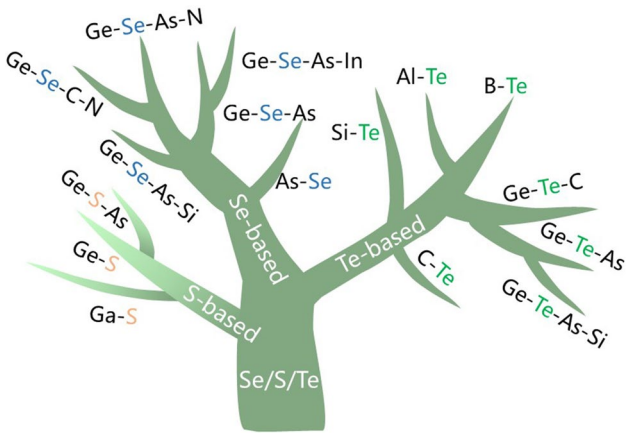

Fig. 4 OTS material tree. The tree depicts three material systems, including Te-, Se-, and S-based ones

3.1 Se-based OTS

Selenium (Se) is the number 34 element in the periodic table (Fig. 5a), with an atomic radius of 1.20 Å. Se-based OTS materials, in which the Se element has the highest concentration, often combine with Ge to form Ge–Se alloys. Ge–Se compounds have been widely reported as OTS matrix for mechanism analysis, doping, and compositional optimization [41–47]. Ge–Se exhibits a high crystallization temperature, with GeSe having a crystallization temperature of 350 °C (Fig. 5b) and further rising up to 600 °C with higher Se content [38, 39]. Since elemental Se has a large mobility gap of ~ 2 eV, the Ge–Se-based materials have a mobility gap ranging from approximately 1–2 eV (Fig. 5c) [46], demonstrating $< 10^{-7}$ A low leakage current and $> 10^{8}$-cycle high endurance (Fig. 6b, h). The trap states of Ge–Se alloy are located at 0.42–0.56 eV below the conduction band edge using a Poole–Frenkel fitting [38]. The Ge–Se bond has a short bond length of ~ 2.38 Å and thereby high bond energy of 234.5 kJ mol^{-1} [32]. Thus, Se-based OTS materials generally exhibited large V_{th}, > 2 V@10 nm thick, which would further increase with higher Se concentration (Fig. 6d) [38].

When optimizing the Ge–Se system, the overall objective is to construct a stable amorphous network, enhance thermal stability, reduce leakage current, and, to some extent, lower the V_{th}. Researchers have extensively investigated the improvement of Ge–Se system performance through doping engineering. For instance, Avasarala et al. introduced N into

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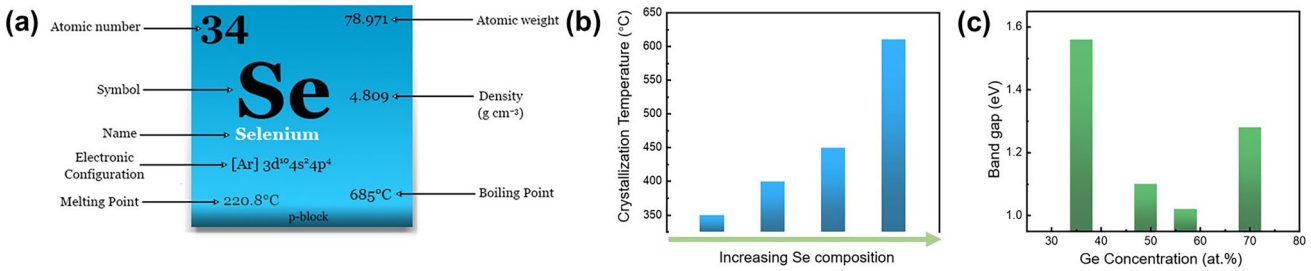


Fig. 5 Elemental Se and Ge–Se properties. **a** Element selenium's properties. **b** Crystallization temperatures (*Tc*) [38] and **c** mobility gap of Ge–Se alloys [39, 40]. Adapted with permission from [39]. Copyright 2011, IOP Publishing

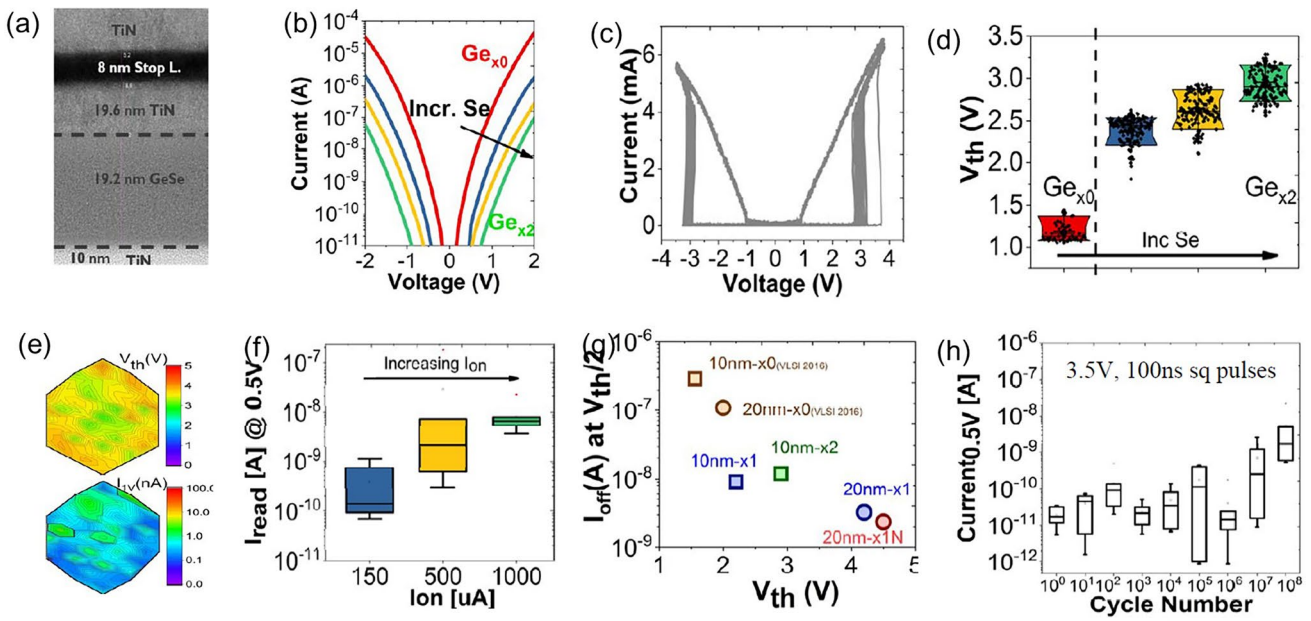
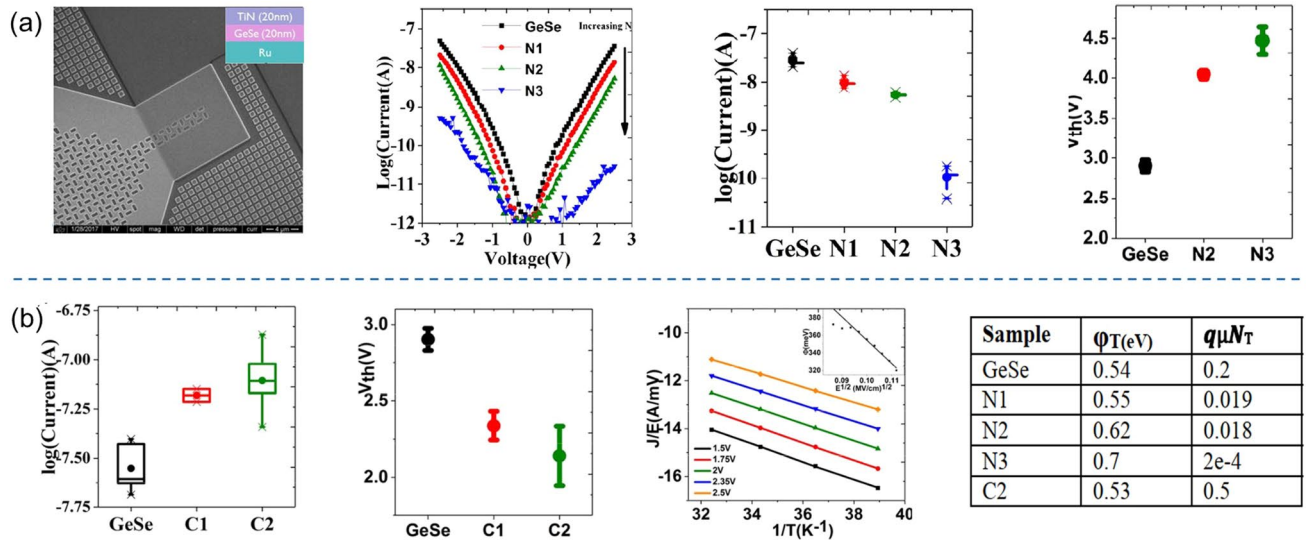


Fig. 6 Ge–Se OTS selectors. **a** Device structure with 50-nm plug. **b** Leakage current. **c** AC *I*–*V* curves. **d** V_{th} increase with higher Se content. **e** V_{th} and I_{off} distributions. **f** I_{on} vs. leakage current. **g** I_{off} comparison and **h** endurance. Adapted with permission from [38]. Copyright 2018, IEEE

Ge–Se to eliminate some of the Ge dangling bonds, resulting in a shift of the mobility edge, hence increased mobility gap, and reduced I_{off} (Fig. 7a) [32]. As the content of N increased from N1 to N3, the trap states became deeper (0.54–0.7 eV), reducing defect density and minimizing leakage current from ~ 5×10^{-8} A to ~ 10^{-10} A, yet causing a sharp increase in V_{th} from ~ 2.8 eV to ~ 4.5 V (Fig. 7a). Moreover, N doping effectively enhanced the thermal stability of the material (> 450 °C). On the other hand, C doping in Ge–Se led to an increase in I_{off} up to ~ 10^{-7} A and a ~ 0.8 V decrease in V_{th} as the content of C reached C2 (Fig. 7b), which differ from N doping. Avasarala et al. believed that the increased density of trap states or introduced C-chain-based gap states after C doping was responsible for the increased leakage and the decreased V_{th} [32].

Similarly, Sb doping decreases V_{th}, and the higher the Sb content (Sb < 22 at.%), the lower the V_{th} (Fig. 8) [48]. In 2021, Keukelier et al. conducted a systematic study on the effects of doping elements on the thermal stability and OTS performance of the Ge–Se system, focusing on Zr (metal), B, Sb (metal-like), C, and N (non-metal) [49]. Their results showed that B doping lowered the crystallization temperature, while Zr doping initially lowered it and then surpassed the pristine material temperature at 5 at.% (Fig. 8b). Sb doping initially increased the crystallization temperature, but started to decrease after reaching 26 at.%. C doping



Sample	φT(eV)	qμNT
GeSe	0.54	0.2
N1	0.55	0.019
N2	0.62	0.018
N3	0.7	2e-4
C2	0.53	0.5

Fig. 7 N- or C-doped GeSe OTS selectors. **a** Device structure with 3 μm×3 μm size; *I–V* curves of N-doped GeSe selector; I_{off} vs. different N contents; V_{th} vs. different N contents. **b** I_{off} vs. different C contents; V_{th} of C-doped samples; T dependence of subthreshold conduction fitting confirming Poole–Frenkel conduction; trap positions and densities. Adapted with permission from [32]. Copyright 2017, IEEE

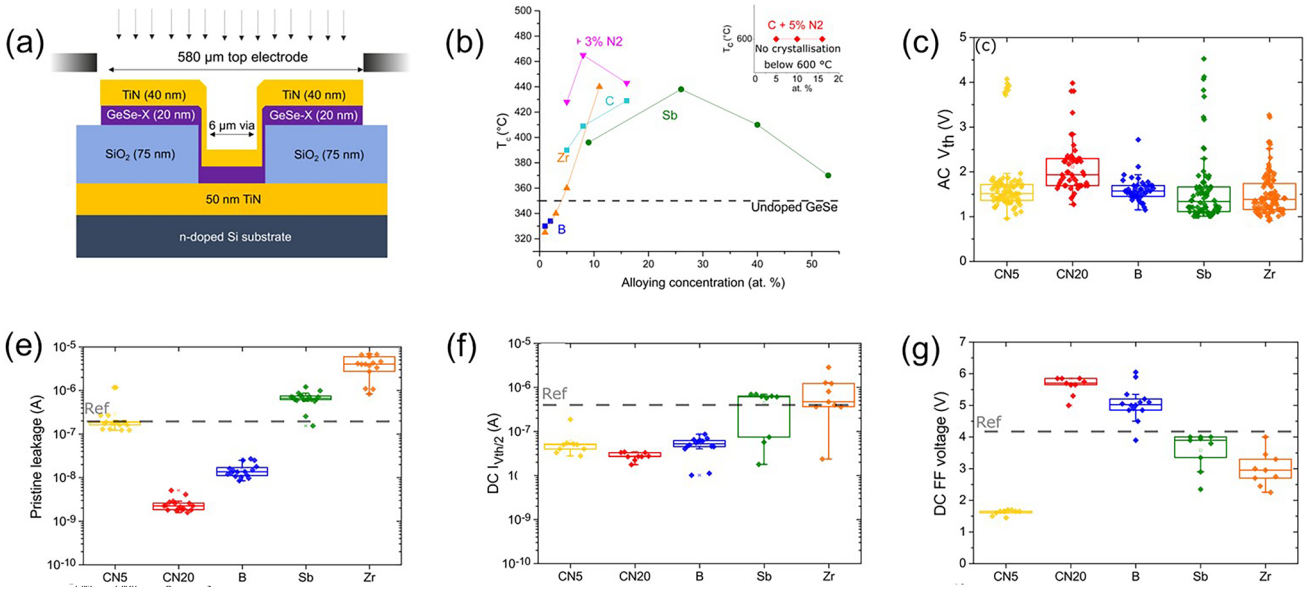


Fig. 8 C/Sb/B/N/Zr-doped GeSe OTS selectors. **a** Device structure with 6 um size. **b** Crystallization temperature T_c. **c** Alternating current (AC) V_{th}. **e** Pristine leakage at 1 V/2 V. **f** I_{off}. **g** V_{ff} voltage. Adapted with permission from [49]. Copyright 2021, AIP Publishing

significantly raised the crystallization temperature, with a temperature exceeding 400 °C at 8 at.%. Further N doping increased the crystallization temperature to 600 °C (Fig. 8b). No matter metallic or metalloid elements are doped, the alternating current (AC) V_{th} of the sample had little difference and remained about 1.5 V (Fig. 8c). *C*/*N* and B doping reduced leakage current, while Sb and Zr doping increased it (Fig. 8e, f). In Ge–Se, Ge–Ge homopolar bonds contributed to leakage current, and N doping reduced homogenization and leakage current. Doping with only N led to excessively high operating voltages, while doping with only C increased leakage current. The most suitable approach was believed to be C and N co-doping. Overall, Sb and Zr contents above 10 at.% modulated the crystallization temperature to exceed

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400 °C. In the study, metal and metalloid elements even decreased the crystallization temperature at low doping concentrations (< 3 at.%), while the non-metal element C effectively increased the crystallization temperature at relatively low doping concentrations. Regarding the impact on electrical characteristics, metal elements were more effective in reducing the V_{th} and V_{ff} (Fig. 8g).

The element As, despite being considered environmentally unfriendly and requiring specific fabrication processes, plays a significant role in the optimization of Ge–Se OTS materials. Most importantly, Ge–Se–As–Si–based OTS material was believed to be the one used in the commercial 3D Xpoint in 2017 [11]. The IBM/Macronix team, focusing on PCM, conducted continuous research on the Ge–Se–As system [50–52]. Cheng et al., by optimizing the content of Ge and As, successfully increased the materials' crystallization temperature to over 450 °C and achieved a low I_{off} of 10^{-10} A, a large J_{on} of 7.9 MA cm^{-2} and the device endurance exceeding 6.9×10^{11} cycles (Fig. 9a) [50]. Using this selector, 1S1R (OTS + PCM) structure was successfully fabricated, demonstrating a ~ 2 V memory window, a 300 ns speed and > 10^{12}-cycle read endurance (Fig. 9b). Subsequently, the team further improved the Ge–As–Se system by doping. The introduction of Si in Ge–Se–As devices extended the endurance to 10^{11}, while doping Te resulted in Ge–Se–As–Si devices with enhanced thermal stability up to 500 °C and endurance reaching 10^{11}. In 2021, they also addressed the trade-off issue among V_{th}, I_{off}, and cycling endurance in B-, C-, and S-doped OTS selectors. Furthermore, In-doped Ge–Se–As OTS devices exhibited low I_{off} (~ 0.1 nA), high endurance (~ 10^{10} cycles), and inhibition of V_{th} drift, while minimally affecting V_{th} and I_{off} [52].

In terms of fabrication techniques, in 2023, Jun et al. employed the atomic layer deposition (ALD) process to fabricate Ge–Se–S-based OTS devices [53]. The novel Ge–Se–S material exhibited a slightly larger V_{th} drift compared to $GeSe_2$. However, it demonstrated several advantages, including a lower I_{off}, and a smaller V_{th} fluctuation up to 10^6 cycles. The successful application of the ALD process in the fabrication of Ge–Se system OTS devices is expected to contribute to the further miniaturization of 3D cross-point (Xpoint) memory and the realization of 3D Vertical memory in future.

Table 2 summarizes device performances of Ge–Se-based OTS selectors. Clearly, Ge–Se-based OTS selectors present thermal stability of > 350 °C, J_{on} ranging from 0.1 to 23 MA cm^{-2}, I_{off} ranging from 10^{-7} to 10^{-10} A, V_{th} ranging from 1.4 to 4 V, V_{hold} ranging from 0.5 to 1.8 V, endurance ranging from 10^6 to 10^{11} cycles.

3.2 Te-based OTS

Tellurium (Te) is the 52nd element on the periodic table, with an atomic radius of 1.4 Å (Fig. 10). Te exists in the trigonal crystalline state at room temperature since it has an ultralow crystallization temperature of −10 °C [58]. Trigonal Te shows a band gap from 0.33 eV to 1.43 eV as the thickness decreases, and has a melting point of approximately

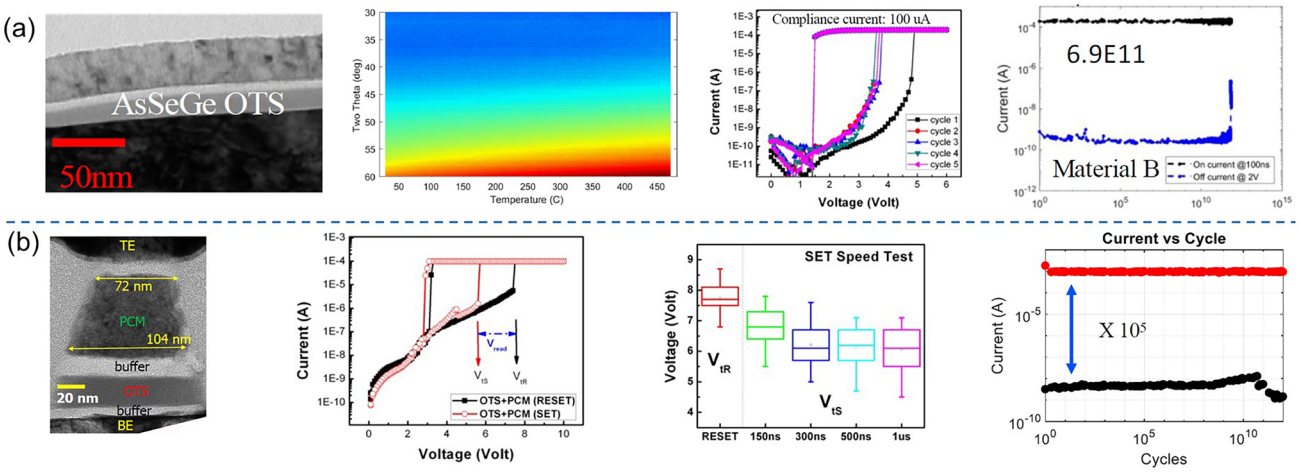

Fig. 9 Ge–Se–As OTS and 1S1R cells. **a** OTS device with 350-nm plug; > 450 °C thermal stability; *I–V* curves showing 3.5 V V_{th} and ultralow I_{off} (131 pA@2 V); 6.9×10^{11}-cycle endurance. **b** 1S1R stacking structure; *I–V* curves showing ~ 2 V memory window; 300 ns speed and > 10^{12}-cycle read endurance. Adapted with permission from [50]. Copyright 2021, IEEE

Table 2 Performance summary and comparison of Se-based OTS devices

Materials	Feature size/nm	Selectivity	J_{on}/MA cm^{-2}	I_{off}/A	V_{th}/V	V_{hold}/V	Speed/ns	Endurance	Thermal stability/°C
GeSe [54]	50	10^3	23	10^{-7}	~1.4	~0.5	~2	10^8	~350
Ge–Se–N [32]	50	10^5	23	2×10^{-9}	~4	~1	–	10^8	>475
Ge–Se–Si [43]	200	10^3	1.6	10^{-7}	~2.4	~1.2	~20	5×10^6	>375
Ge–Se–As [50]	350	10^5	7.9	1.3×10^{-10}	~3.5	~1.2	~10	6×10^{11}	~450
Ge–Se–Sb–N [31]	–	10^4	1.4	10^{-9}	2.2	0.76	–	10^6	<475
Ge–Se–As–Te–Si [55]	350	10^4	0.44	1.9×10^{-9}	~2.2	~1.5	~50	$>10^{10}$	>350
Ge–Se–As–In [52]	350	10^6	0.1	$\sim1\times10^{-10}$	3.7	~1.8	–	$<10^{10}$	~350
Ge–Se–S [53]	50	10^4	~5	4×10^{-8}	~3.2	–	–	$>10^6$	–

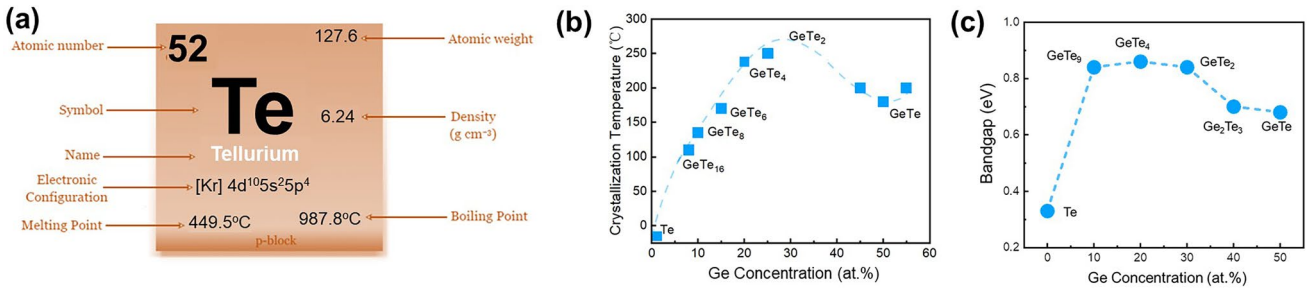

Fig. 10 Elemental Te and Ge–Te properties. **a** Element tellurium's properties. **b** Crystallization temperatures (*Tc*) [56] (Adapted with permission from [56]. Copyright 1986, AIP Publishing) and **c** the mobility gap [57] (Adapted with permission from [57]. Copyright 1974, Elsevier) of Ge–Te alloys, respectively

450 °C [59]. Te plays a significant role in the development of OTS materials, as evidenced by the first discovered As–Te–I OTS system, as well as the pioneering Te–As–Si–Ge OTS materials. However, despite the extensive exploration of various ternary and even binary Te-based chalcogenides exhibiting OTS behavior, the intrinsic properties of Te as a standalone element have long been overlooked. It wasn't until 2021 that Shen et al. discovered elemental Te selector switch based on the novel crystal-liquid–crystal phase transition mechanism, intrinsically differing from conventional OTS selectors [60]. Pure-Te device exhibited a large drive current density > 11 MA cm^{-2}, a rather high selectivity of 10^3, a $I_{off} < 10^{-6}$ A, and a fast switching speed < 20 ns [60, 61]. The ~0.95 eV Schottky barrier formed at Te/TiN interface enabled an I_{off} of 0.4 μA, which reduced to ~50 nA after 35 at.% Zn-doping and further to 88 pA after 50 at.% Mg-doping with a large 3 eV mobility gap. Noticeably, resembling the elemental Te cell, the Zn/Mg-doped Te layer remained in the crystalline state in the off-state [62, 63].

Binary Te-based systems have attracted attention due to their simplicity in composition and environmental friendliness. Among binary Te OTS materials, Ge–Te alloys is the earliest studied and popular OTS matrix. In 2012, Anbarasu et al. first reported that $GeTe_6$ cell surprisingly presented an OTS behavior, rather than an OMS one found in typical GeTe device, with 5 ns fast switching speed and 0.65 mA I_{on} and 600-time cycles (Fig. 11a) [64]. Then $GeTe_4$ OTS materials were also found by Velea et al. (Fig. 11b) [65], the V_{th} of which increased from 1.2 eV to 1.55 V and the on/off ratio degraded from 5×10^3 to 10^2 (compared to $GeTe_6$). Since the low mobility gap width of Ge–Te materials ranged from 0.33 to 0.9 eV (Fig. 10d), Ge–Te OTS selector presented a low V_{th} of < 1.7 V@ 20 nm thick. Ge–Te devices exhibited good consistency among different device units, with low fluctuations observed during multiple tests of the same device unit. However, the narrower mobility gap also led to a large leakage current > 10^{-8} A. Additionally, as pure Te crystallizing at −10 °C, the highest crystallization temperature was found to only ~260 °C even increasing Ge content to 33.3 at.% ($GeTe_2$) (Fig. 10b), far lower than the 400–450 °C required for the BEOL process. It also means that the Ge–Te films are more likely to crystallize during

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switching, which is one of the main reasons for the reduced endurance of the OTS selector (< 1000 cycles) [64]. From a bond energy perspective, the Te atomic radius is 1.4 Å, and the Ge–Te bond energy is 192 kJ mol^{-1} [66], indicating longer bond lengths and weaker bond energies. This makes it less capable of withstanding high temperatures and large current.

In order to solve the problem of insufficient thermal stability of $GeTe_6$ itself, Velea et al. proposed three optimization paths: reducing Te content, adding Si element, and directly replacing Ge with Si to form Si–Te system [65] (Fig. 11b). The reduction of Te content alone cannot significantly increase the crystallization temperature; in that report, the maximum increase was only 45 °C, and there was a clear bottleneck for further improvement. After 2 at.% Si doping, it exhibited OTS switching behaviors in current-limiting tests [67], whereas non-volatility occurred as the Si content exceeds 5 at.% [68]. Besides, to improve the thermal stability and reduce the I_{off}, in 2021, Wu et al. [35] doped C into the Ge–Te alloy, which sharply extended the device lifetime to > 10^{11}-cycle and exhibits an I_{off} < 5 nA, a switching speed about 5 ns, and a V_{th} of 1.3 V (Fig. 12a). In the same year, Wang et al. [69] also investigated 5 at.% C-doped Ge–Te OTS selector, presenting I_{on} = 2 mA, I_{off} = 2 nA, 8.5 ns on-speed, and > 10^7 cycles endurance (Fig. 12b).

Ambrosi et al. from TSMC further incorporated N into the Ge–Te–C OTS materials to improve the thermal stability above 400 °C [70], enabling even smaller performance fluctuations, reducing parameter dispersion such as V_{th} after multiple operation, and exceeding 10^{11} cycles (Fig. 13a). The further introduction of Si elements into the system enhanced the robustness of the device. The thermal stability and high-current tolerance of the Ge–Te–C–N–Si system were further enhanced. The device's thermal stability could be improved to above 450 °C, and the voltage drift was reduced compared to the Ge–Te–C and Ge–Te–C–N systems, resulting in significantly improved device reliability with endurance > 10^{10} cycles (Fig. 13b). Additionally, by controlling the Ge content, modulation of defect states in the Ge–Te–C–N–Si system could effectively reduce the difference between V_{ff} and V_{th} within a specific compositional range, achieving a "firing-free" effect [71] (Fig. 13b). This optimization further reduced the requirement for *I/O* voltage in application scenarios and facilitated the application of OTS devices in more advanced process nodes.

Besides C/N/Si doping in Ge–Te OTS cells, the toxic As elements were often incorporated. In 2019, Garbin et al. provided a comprehensive analysis of the effects of the As/Te ratio, Ge and Si content in the Ge–Te–As–Si system on device performance (Fig. 14). Increasing the As/Te ratio raised the crystallization temperature [72]. The addition

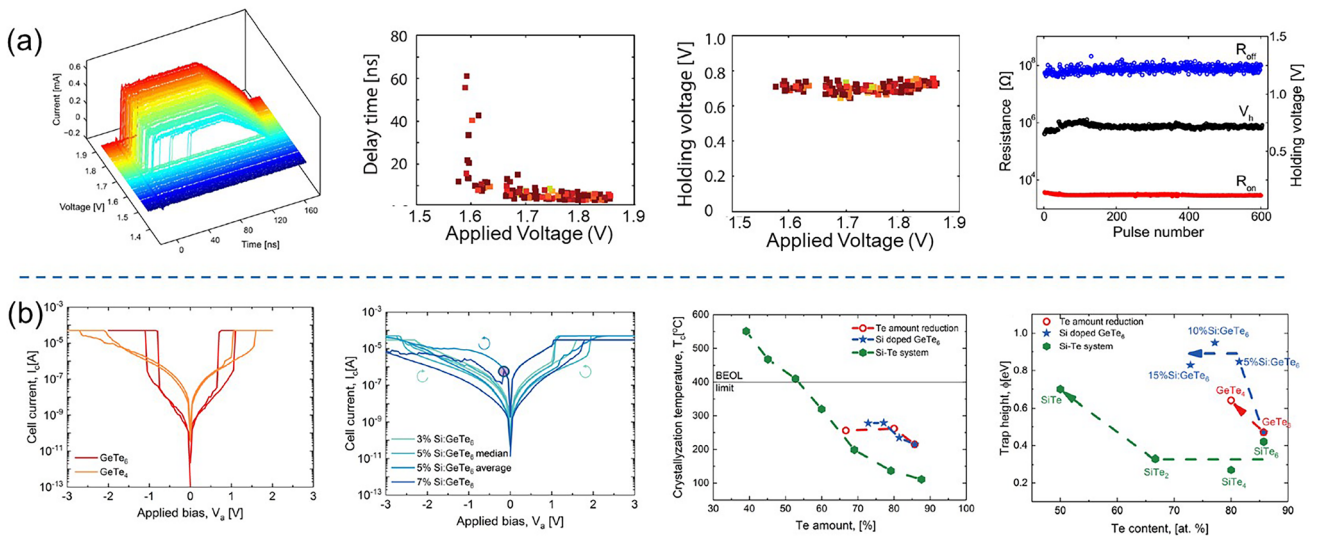

Fig. 11 Ge–Te and Si-doped Ge–Te OTS selectors. **a** Time-resolved measurement, switching speed, V_{hold}, and endurance of $GeTe_6$ OTS cells. Adapted with permission from [64]. Copyright 2012, AIP Publishing. **b** DC *I–V* curves of $GeTe_4$ and $GeTe_6$ cells; DC *I–V* curves of Si-doped $GeTe_6$ cells; Crystallization temperature and trap positions of Ge–Te, Si-doped $GeTe_6$, and Si–Te materials [64, 65]. Adapted with permission from [65]. Copyright 2017, Springer Nature

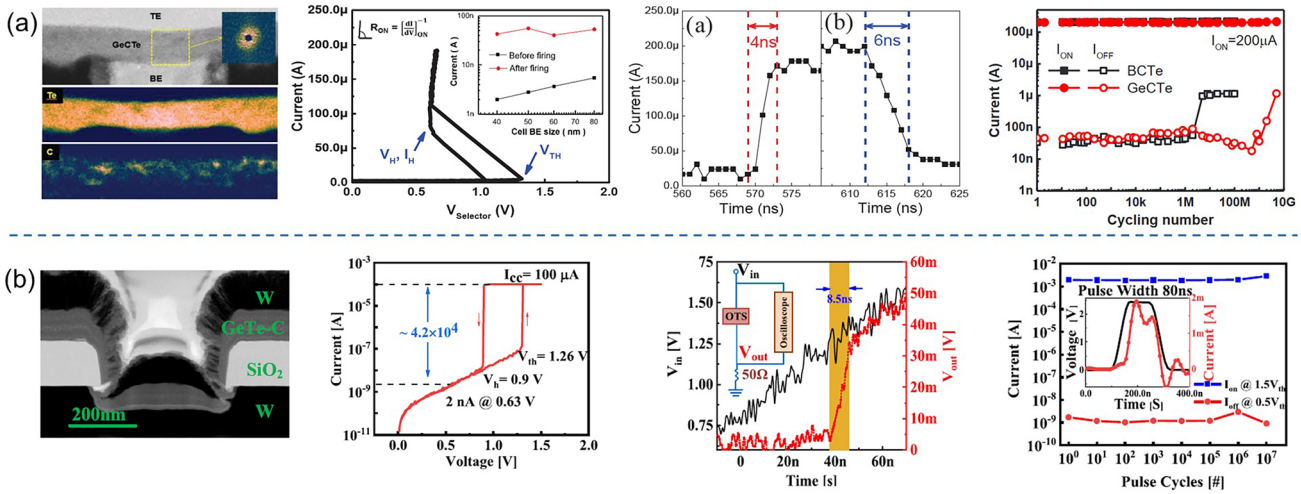

Fig. 12 Ge–Te–C OTS selectors. **a** Device structure (30-nm plug), AC *I–V* curves, switching speed, and endurance of Ge–Te–C OTS cells reported by Wu et al. [35]. **b** Device structure (250-nm BE), DC *I–V* curves, on-switching speed, and endurance of Ge–Te–C OTS cells reported by Wang et al. Adapted with permission from [69], Copyright 2021, IEEE

of Ge to AsTe reduced the mobility gap, and when the Ge content in Ge–Te–As exceeded 20 at.%, the crystallization temperature increased to 450 °C. However, the mobility gap decreased and leakage current increased. The addition of Si increased the mobility gap, raised the crystallization temperature, increased the threshold voltage (V_{th}) to a range of 2.3–2.9 V, and reduced leakage current to 10 nA. In the Ge–Te–As–Si system, strong bonds were formed, resulting in a temperature-stable amorphous network with excellent endurance (10^{11} cycles).

Lee et al. further enhanced the thermal stability to above 500 °C by introducing nitrogen (N) into the Ge–Te–As–Si and solved the performance degradation with repeated cycling and reliability after BEOL process (Fig. 15) [73]. A I_{on} of 0.1 mA was obtained, which were found to be size-dependent. For a 30 nm cell, a $J_{on} > 11$ MA cm^{-2} was

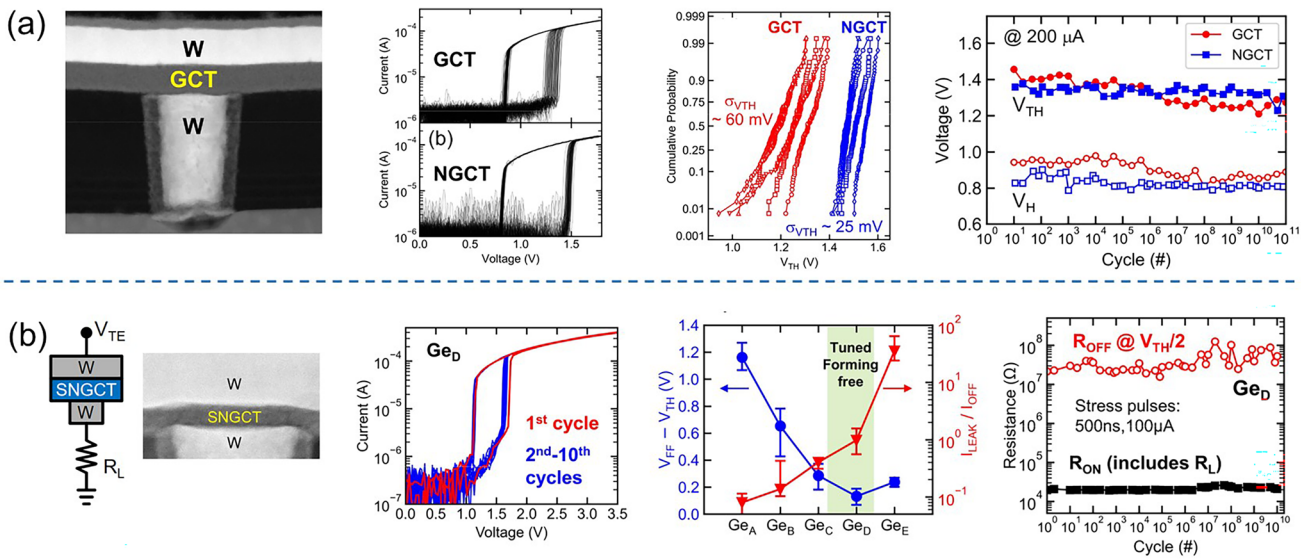

Fig. 13 Ge–Te–C–N (**a**) and Ge–Te–C–N–Si (**b**) OTS selectors. **a** Device structure of a Ge–Te–C–N OTS cell (32–72-nm plug); 100 DC switching cycles; Cumulative probability plot of V_{th}; Endurance. Adapted with permission from [70]. Copyright 2021, IEEE. **b** Device structure of a Ge–Te–C–N–Si cell (~40-nm plug); DC *I–V* curves after repeated operation; Firing-free optimization plot showing firing-free behavior in Ge_D composition; Endurance. Adapted with permission from [71]. Copyright 2022, IEEE

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found. Their cycling performance was shown to be greater than 10^8 cycles. Also, they demonstrated a 1S1R memory cell using a Ta_2O_5/TaO_x resistance memory with the GeTe-AsSiN selector device.

Beside the Ge–Te-based OTS materials mentioned above, there are some binary Te-based OTS materials worth mentioning, including Si-doped, C-doped, B-doped, and Al-doped Te; most of them were first reported by Kazuhiro Ohba and Hiroaki Sei from Sony corporation in 2015 [74]. In their filed OTS patents, they also investigated N, O, Mg, Ga, Y etc. incorporation, for thermal stability enhancement and leakage current reduction, and multi-element doping. They further noticed that the insertion of 2–5 nm high-resistance layer between the OTS layer and electrode, like SiO_x, AlO_x, MgO_x, SiN, and HfO_x, could greatly reduce the I_{off} to sub-nA and even pA. For Si–Te OTS materials, Velea et al. mentioned the crystallization temperature of Si–Te system increased significantly with the decrease of Te content, it could reach 400 °C when Te < 50 at.% [65]. Similar results were found in Koo et al.'s work [75]. The difference was that the electrical performance of Si–Te reported in the former paper was seriously degraded, the selectivity of other Si–Te components was less than 5 except for $SiTe_6$ (~ 100), while Koo et al. reported that Si–Te device had good performance, including an I_{on} of 5×10^{-4}A, I_{off} of ~ 1 nA, thermal stability up to 400 °C, and endurance up to 10^8 cycles.

The C–Te system is another Te-based OTS material that has been extensively reported recently. In 2018, Chekol et al. chose carbon (C) as a component in the C–Te OTS device [77], which had a smaller atomic radius compared to Ge and Si. The C–Te OTS device exhibited a switching ratio greater than 10^5, a current density higher than 11 MA cm^{-2}, an I_{off} current of approximately 1 nA, high endurance of around 10^9 cycles, and thermal stability exceeding 450 °C (Fig. 16b). The V_{th} of C–Te was relatively small ($V_{th} = 0.64$ V, $V_{hold} = 0.36$ V). C–Te was stable when the C content was between 25 and 55 at.%. As the C content increased, V_{th} decreased, while leakage current increased. In 2018, Yoo et al. reported the B–Te system [78], which exhibited a selectivity of 10^5, I_{on} of 5×10^{-4}A, I_{off} less than 10 nA, thermal stability up to 450 °C, and endurance of 10^8 cycles (Fig. 16b). In the same year, Yoo et al.'s comprehensive research showed that in B–Te and Al–Te-based devices [76], the decrease of Te ratio resulted in increased V_{th} and decreased I_{off} (Fig. 16d). The endurance of devices based on C–Te and B–Te could switch > 10^8 cycles in maintaining low I_{off}, while the Al–Te-based device showed I_{off} degradation after 10^7 cycles (Fig. 16d).

Table 3 summarizes the device performances of Te-based OTS selectors. Te-based OTS selectors present a J_{on} ranging from 0.44 MA cm^{-2} to 55 MA cm^{-2}, an I_{off} ranging from 10^{-7} A to 10^{-9} A, a V_{th} ranging from 0.75 V to 2.2 V, and a V_{hold} ranging from 0.3 V to 1.5 V, and an endurance ranging

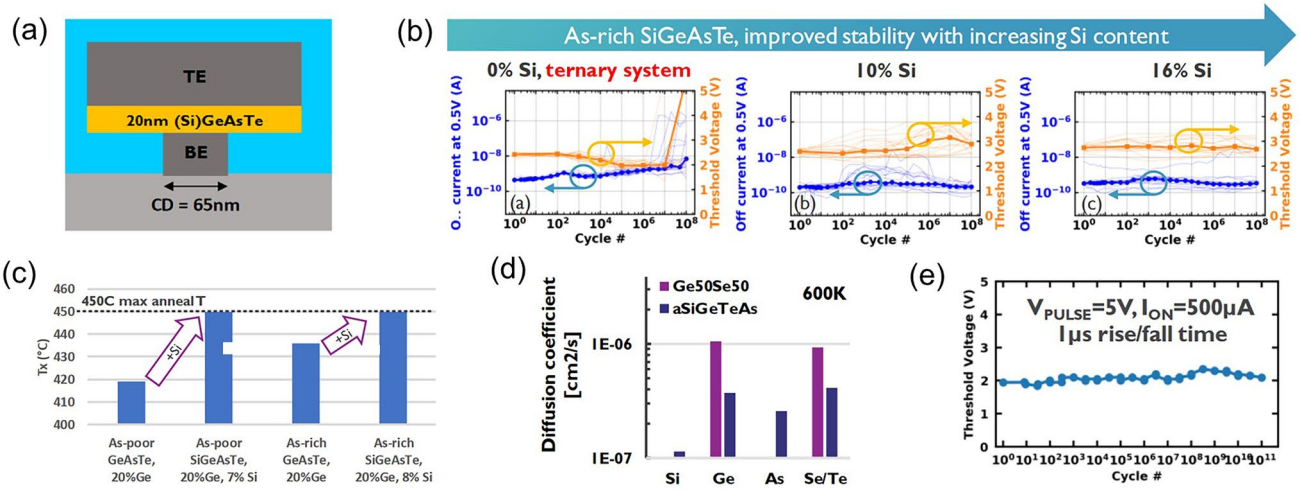

Fig. 14 Ge–Te–As OTS selectors. **a** Device structure (65-nm plug). **b** Endurance of As-rich Ge–As–Te–Si OTS devices with different Si content. **c** Crystallization temperature, moving from Ge–Te–As to Ge–Te–As–Si system increases > 450 °C. **d** Comparison of calculated element diffusion coefficient at 600 K for GeSe and Si–Ge–As–Te. **e** Endurance of 10^{11} cycles achieved Ge–Te–As. Adapted with permission from [72]. Copyright 2019, IEEE

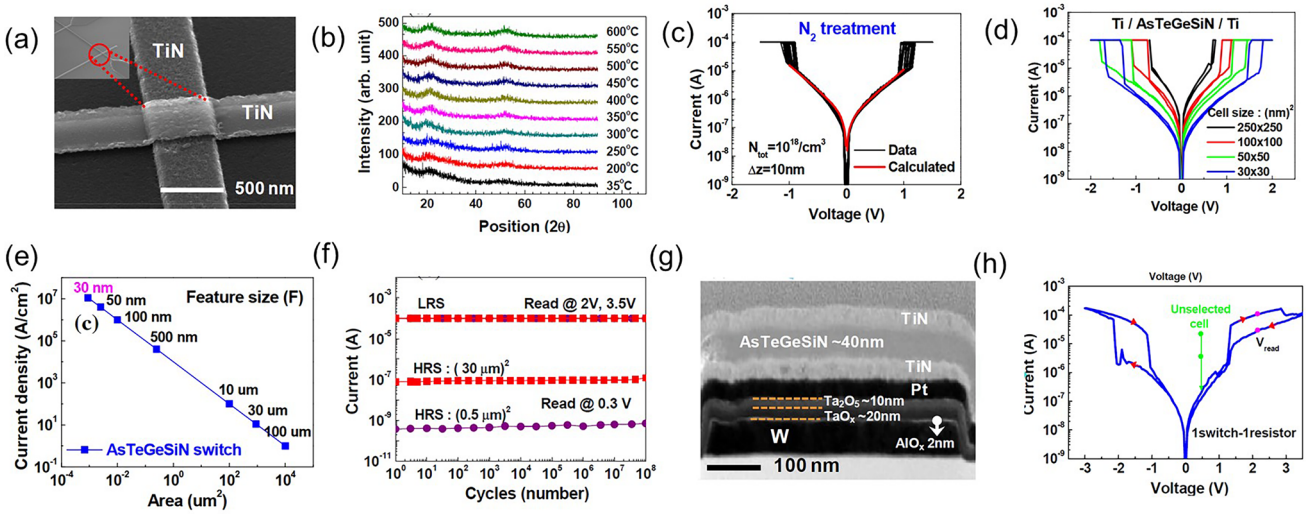

Fig. 15 Ge–Te–As–Si–N OTS selector and 1S1R cell. **a** Device structure with 30 nm–100 um size. **b** Thermal stability above 600 °C. **b** DC *I–V* curves. **c** DC *I–V* curves of the selector with varying sizes. **e** Scaling behavior. **f** Endurance. **g** 1S1R structure with Ta_2O_5/TaO_x memory cell. **h** DC *I–V* curves of the 1S1R cell. Adapted with permission from [73]. Copyright 2012, IEEE

from 600 to 10^{11} cycles. Although Ge–Te OTS materials show lower than 250 °C thermal stability, the incorporation of light atoms (with a smaller radius) or the replacing of Ge by these atoms, forming strong bond and robust amorphous network, significantly improve the thermal stability above 400 °C, enabling the withstanding of the BEOL process in the memory fabrication.

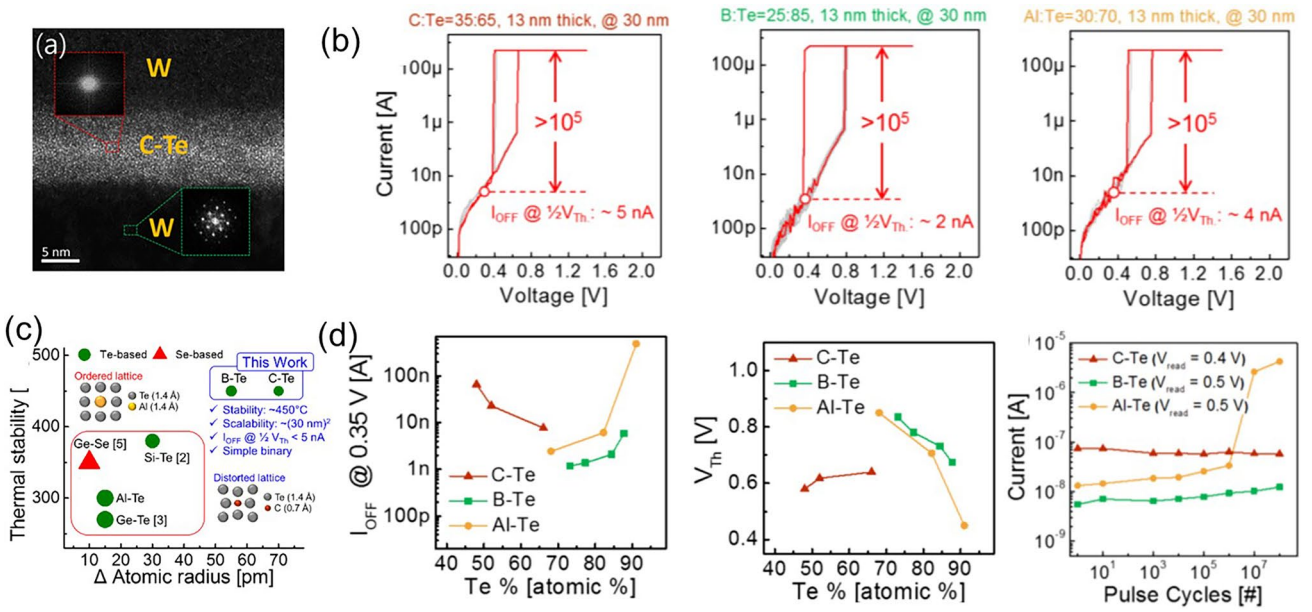

Fig. 16 C–Te, B–Te, and Al–Te OTS selectors. **a** Device structure with 30–150 nm size. **b** DC *I–V* curves. **c** Relation between thermal stability and atomic radius difference. **d** I_{off}, V_{th} and endurance. Adapted with permission from [76]. Copyright 2018, IEEE

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3.3 S-based OTS

As the most representative element in the chalcogen, the 16th element sulfur (S) has been the subject of numerous investigations, regarding its crystal structure [84–89], electronic structure [84, 85, 90–92], thermodynamic properties [84], and other physical characteristics (Fig. 17a). The crystallization temperature of pure S is about 0 °C and the melting point is 115 °C [93]. In 2020, Jia et al. first reported S-based OTS materials [66], GeS, and then Ge–S alloys were systematically studied. Since the atomic radius of S atoms was just 0.88 Å, > 0.3 Å smaller than Se and Te atoms, the Ge–S compounds exhibited high crystallization temperatures, 380 °C for GeS and exceeding 600 °C for GeS_2 [92]. The mobility gap of Ge–S system increased with an elevated concentration of S, for S-rich Ge–S, the mobility gap ranged from 2.6 V to 3.4 eV and it could reach 3.8 eV in pure S (Fig. 17b, c) [94]. Consequently, Ge–S-based OTS device exhibited a rather low I_{off}. The Ge–S bond energy is 266 kJ mol^{-1} [66], indicating a strong bond that enables the material to withstand higher temperatures and larger passing current.

In 2020, Jia et al. discovered novel GeS OTS devices from the perspective of constructing a more stable amorphous system [66]. The device consisted of W bottom electrode with a diameter of 190 nm, Al top electrode, and the 10-nm-thick GeS layer sandwiched between them (Fig. 18a). Due to strong Ge–S bond and wide mobility gap of GeS (~ 1.5 eV), the GeS selector exhibited high drive current ~ 10 mA (J_{on} = 34 MA cm^{-2}) and low leakage current ~ 10 nA (Fig. 18b). The V_{th} in the selector was ~ 3.2 V, while the V_{hold} was ~ 0.3 V (Fig. 18b). The GeS OTS device demonstrated favorable bi-directional selectivity and scalability (Fig. 18c), with a high switching speed (t_{on} ~ 10 ns, t_{off} ~ 100 ns) (Fig. 18d), an on/off ratio of approximately 10^6 and endurance exceeding 10^8 (Fig. 18e). In terms of thermal stability, the device maintained switching performance after annealing at 350 °C. Considering the trade-off between selectivity ratio and high driving current, GeS devices demonstrated remarkable performances, when compared to Se and Te selectors (Fig. 18f).

It is worth noting that the top electrode in that paper was made of Al, which would cause the diffusion of Al atoms and form conductive channels in the material layer, thus affecting the switching process. In the subsequent report [95], the author reported GeS OTS devices with both TiN

Table 3 Performance summary and comparison of Te-based OTS devices

Materials	Feature size/nm	Selectivity	J_{on}/MA cm^{-2}	I_{off}/A	V_{th}/V	V_{hold}/V	Speed/ns	Endurance	Thermal stability/°C
B–Te [76]	30	10^5	~ 55	~ 10^{-8}	~ 0.75	~ 0.3	~ 2	10^8	> 450
Si–Te [75]	100	10^6	10	~ 1×10^{-9}	~ 1.2	~ 1	~ 2	10^8	> 400
C–Te [77]	30	10^5	11	5×10^{-9}	~ 0.64	~ 0.36	~ 2	> 10^8	> 450
$GeTe_6$ [64]	60	10^5	~ 1.8	–	~ 1.6	~ 0.7	–	600	–
Ge–Te–C [35]	30	10^5	~ 24.8	3×10^{-9}	1.32	0.62	–	> 10^{11}	< 300
Ge–Te–C–N [70]	~ 40	> 10^4	~ 8	3×10^{-9}	~ 1.4	~ 1	–	> 4×10^{11}	400
Ge–Te–Si–N–C [34]	~ 32	10^4	12.4	~ 10^{-8}	1.7	~ 1	–	> 10^{10}	> 450
Ge–Te–As [79]	110	10^5	17	3×10^{-8}	~ 0.75	~ 0.6	~ 10	–	–
Ge–Te–As–Si–N [80]	30	10^3	11	~ 10^{-7}	~ 1.8	~ 1.5	~ 4	10^8	> 450
Ge–Te–As–Se–Si [51]	350	10^4	0.44	1.9×10^{-9}	~ 2.2	~ 1.5	~ 50	10^{10}	> 350

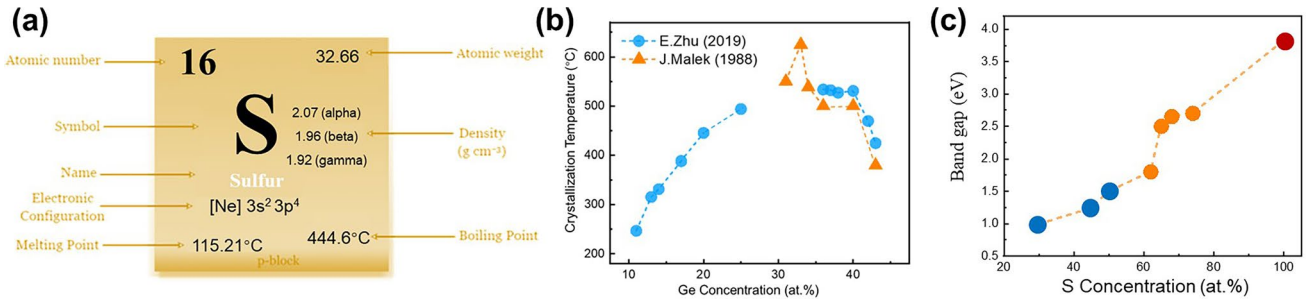

Fig. 17 Elemental S and Ge–S properties. **a** Element sulfur's properties. **b** Crystallization temperatures and **c** the mobility gap of Ge–S alloys [81–83]

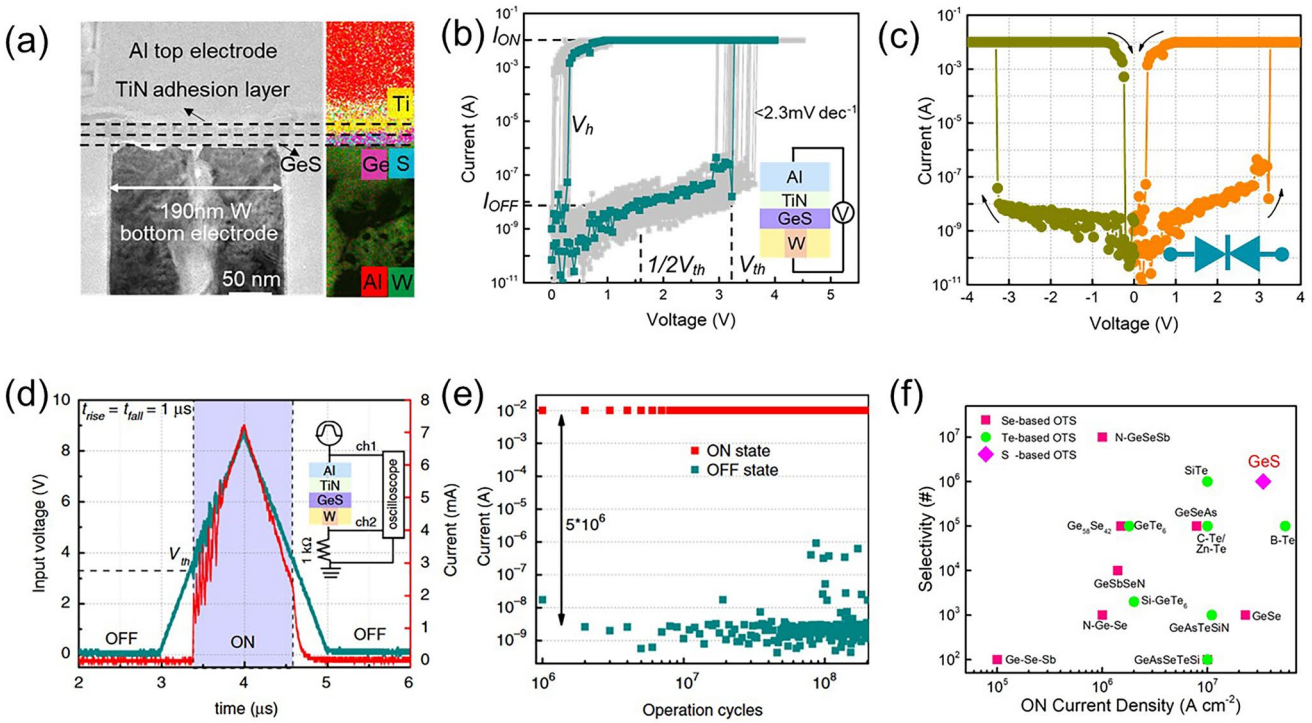

Fig. 18 GeS OTS selectors. **a** Device structure with 190-nm plug. **b** DC *I–V* curves. **c** DC bi-directional curves. **d** AC speed test. **e** Endurance > 10^8. **f** Comparison of selectivity and J_{on} of reported OTS devices [66]. Adapted with permission from [66]. Copyright 2020, Springer Nature

top/bottom electrodes (Fig. 19a). The GeS device with TiN electrodes (Fig. 19a) showed a lower V_{th} of 1.75 V and a higher V_{hold} of 0.75 V (Fig. 19b, c), the selector exhibited an I_{on} of 1 mA, and large current density ~ 35.4 MA cm^{-2} in 60 nm-sized devices (Fig. 19d). Noticeably, the off-speed in this selector is more than 10 times faster (~ 7 ns) than the previous one (Fig. 19e), indicating that the diffusion of Al slowed down the switching process (also increased the I_{on}), but this effect did not lead to significant changes in the main switching mechanism of the device, which was still an OTS switching. Compared with other selectors, GeS OTS selector still had obvious advantages in the drive current density and could be further improved with the feature size scaling down (Fig. 19f).

In 2023, Wu et al. reported the Ge–S–As OTS device with various As concentrations and systematically elaborated the

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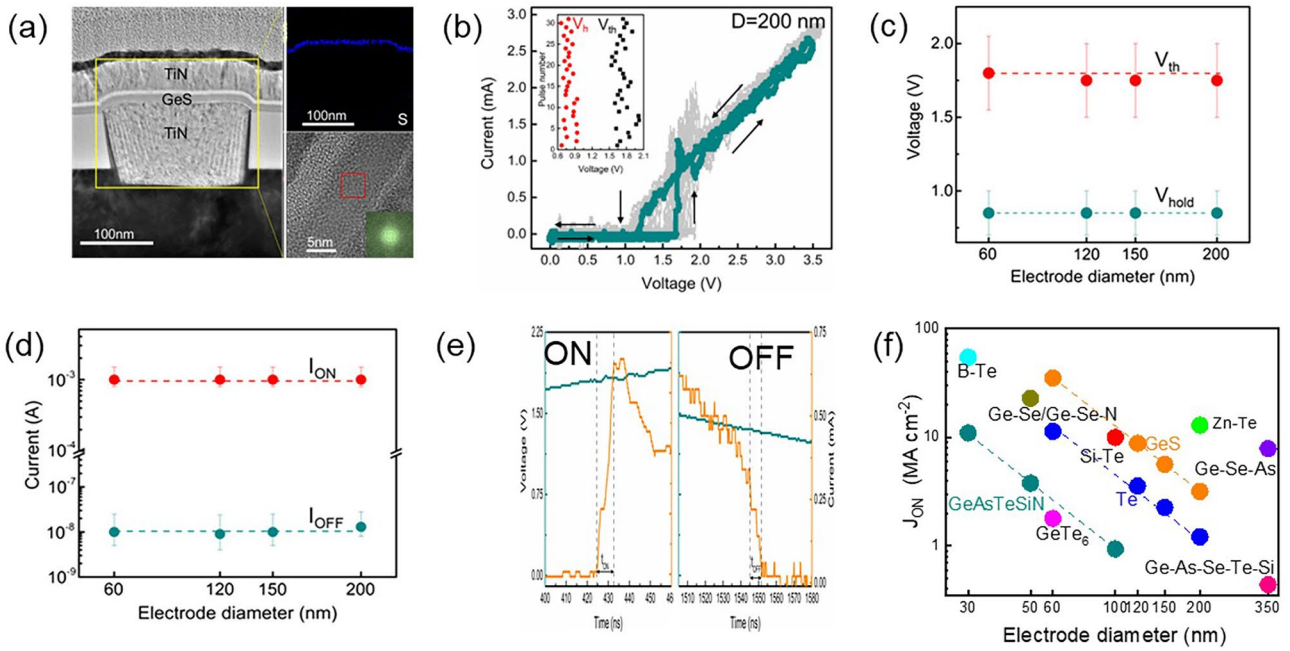

Fig. 19 GeS OTS device with TiN electrodes. **a** Device structure with 60–200-nm plug. **b** AC *I*–*V* sweeps. **c**, **d** V_{th}, V_{hold}, I_{on} and I_{off} dependence on the electrode size. **e** On/Off speed; **f** Comparison of the J_{on} of the GeS OTS cell with other Te- and Se-based selectors [95]. Adapted with permission from [95]. Copyright 2021, John Wiley and Sons

key role of As element in OTS switching [96]. They discovered that incorporation of As into GeS brought a more than 100 °C increase in crystallization temperature (> 450 °C) (Fig. 20a, b), improving the switching repeatability and prolonging the device endurance (~ 10^{10} cycles), which was attributed to the strengthened As-S bonds and sluggish atomic migration after As incorporation. The addition of As reduced the leakage current by more than an order of magnitude (Fig. 20e, f) and significantly suppressed the operational voltage drift, ultimately enabling a BEOL-compatible OTS selector with a V_{th} of 2 V, an I_{on} higher than 12 MA cm^{-2}, an on/off ratio over 10^4, a speed about 10 ns, and an endurance approaching 10^{10} cycles after 450 ℃ annealing (Fig. 20h).

In 2021, Kim et al. fabricated GeS_2 and Ge_2S_3-based OTS devices using the plasma-enhanced atomic layer deposition (PE-ALD) [94]. Through comprehensive considerations of factors such as growth temperature and purging time of the $GeCl_4$ precursor, the team discovered that PE-ALD $Ge_{1-x}S_x$, utilizing an H_2S/Ar plasma reactant, exhibited a self-limiting growth behavior within an ALD window. As a result, the team successfully fabricated GeS_2 and Ge_2S_3 films by ALD, which exhibited thermal stability up to 600 °C (Fig. 21a). The 15-nm-thick GeS_2 device exhibited an I_{on} of 0.1 mA, a V_{th} of approximately 5 V and a I_{off} of 20 nA. The trade-off relationship between the V_{th} (1.9–6.2 V) and the normalized I_{off} (20–250 nA) was observed by scaling down the film thickness from 30 to 5 nm (Fig. 21a). Surprisingly, Ge_2S_3 OTS devices required lower V_{th} owing to lower trap density according to the Poole–Frenkel fitting (Fig. 21a).

In 2023, Lee et al. from the same group continued the exploration of $Ge_{1-x}S_x$ series OTS devices [97], which revealed that Ge-rich compositions ($0.2 \le x < 0.5$) exhibited metallic behavior due to Ge crystallization caused by Joule heating. On the other hand, devices with S-rich compositions ($0.5 \le x \le 0.67$) demonstrated OTS behaviors (Fig. 21b). As the S content increased, the material's mobility gap widened from 1.65 eV for Ge_2S to 3.45 eV for GeS_2. Consequently, the devices exhibited increased V_{th} (ranging from 3.4 V to 5 V), reduced I_{off}, with the lowest reaching 1.3 nA (Fig. 21b). The endurance of the devices reached up to 10^9 cycles, and the devices exhibited thermal stability up to 600 °C. Note that mobility gap values of Ge–S alloys in this work was > 1 eV larger than reported film samples which may be due to the material contamination [97].

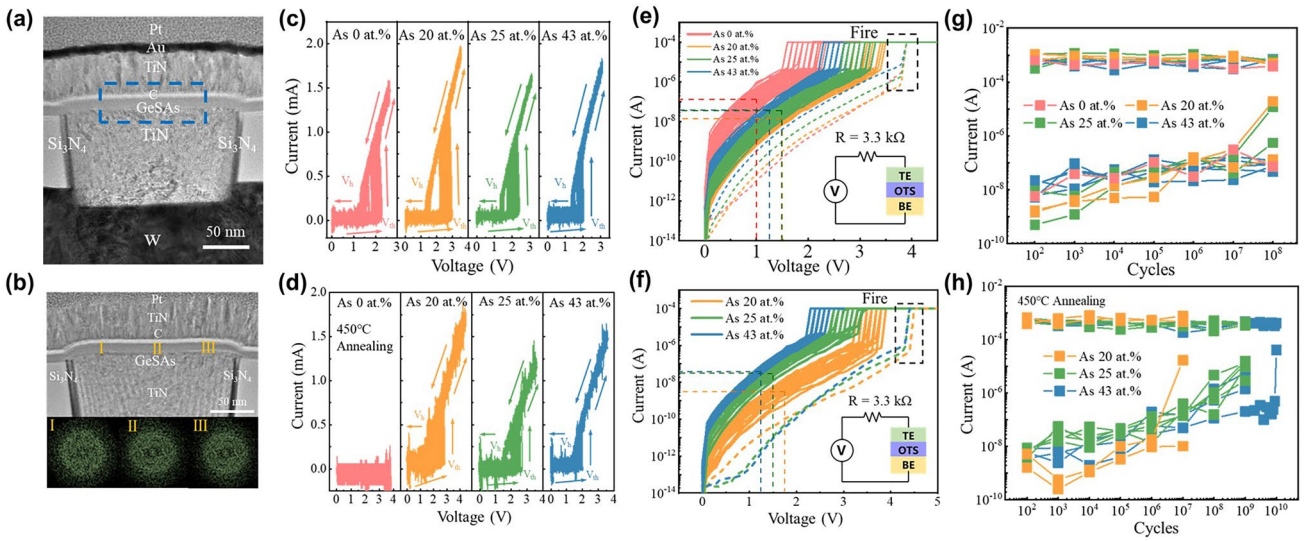

Fig. 20 GeSAs OTS selectors. **a**, **b** Device before/after 450 °C annealing. **c**, **d** *I*–*V* curves of Ge–S–As devices before/after 450 °C annealing. **e**, **f** DC *I*–*V* curves of devices before/after 450 °C annealing. **g**, **h** Endurance performance of Ge–S–As before/after 450 °C annealing. Adapted with permission from [96]. Copyright 2023, Springer Nature

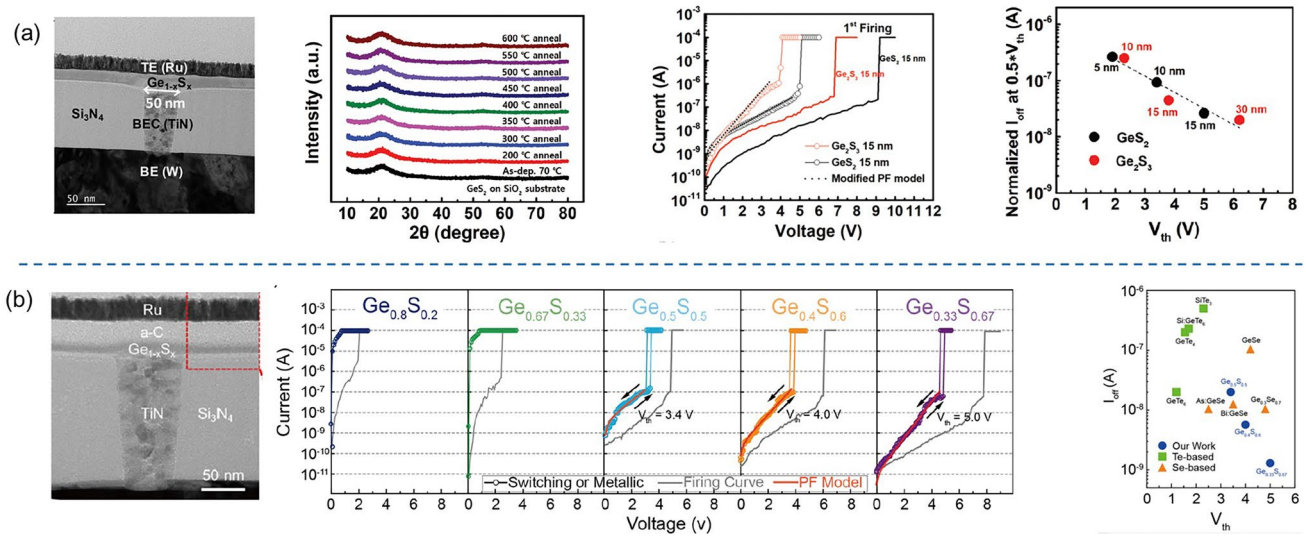

Fig. 21 Ge–S OTS selector. **a** Device structure with 50-nm plug; Thermal stability of GeS_2 above 600 °C; DC *I*–*V* curves of GeS_2 and Ge_2S_3 cells; I_{off}. Adapted with permission from [94]. Copyright 2021, Royal Society of Chemistry. **b** Device structure with 60-nm plug; DC *I V* curves of Ge–S devices; I_{off} and V_{th} comparisons [53, 94, 97]. Adapted with permission from [97]. Copyright 2023, Elsevier

In 2022, Matsubayashi et al. conducted high-throughput calculations to screen environment-friendly ternary OTS materials [98]. The first screening filter was element exclusion to narrow down the combinations. They focused on the 14 elements: B, C, N, Al, Si, P, S, Zn, Ga, Ge, In, Sn, Sb, and Te, the ternary combination of which generated about thirteen thousand compositions (10% atomic fraction step, Fig. 22a). The second screening filter was the glass-transition temperature > 600 K, required for BEOL process, by which about six thousand compositions left. The third screening filter was the 5 valence-electron rule to populate the antibonding state (unstable) and activate the OTS

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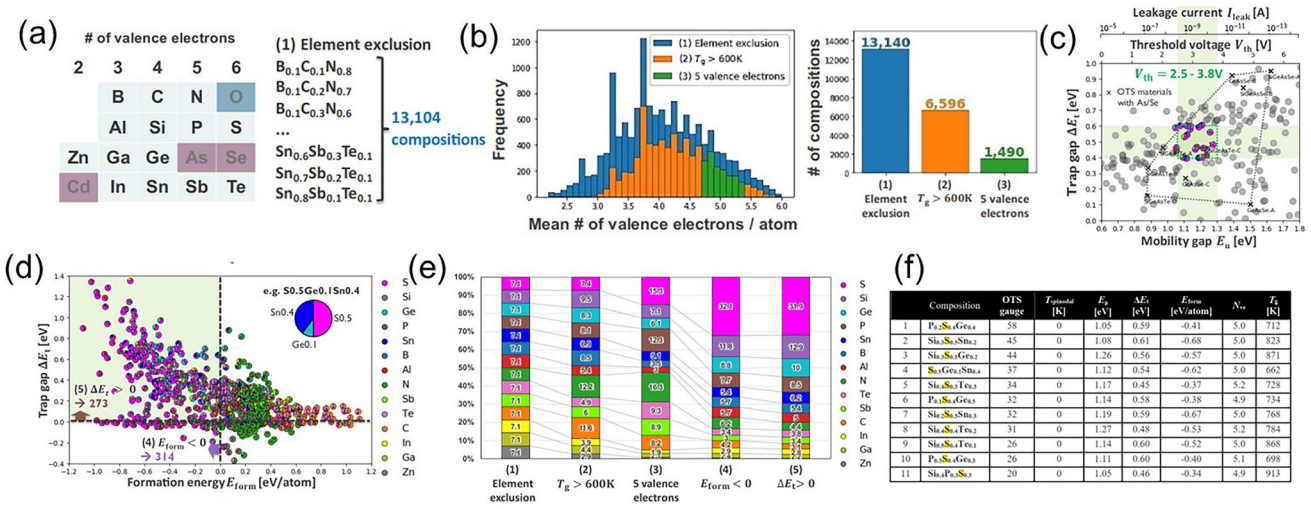

	Composition	OTS gauge	$T_{spinodal}$ [K]	E_g [eV]	ΔE_t [eV]	E_{form} [eV/atom]	N_{ve}	T_g [K]
1	$P_{0.2}S_{0.4}Ge_{0.4}$	58	0	1.05	0.59	-0.41	5.0	712
2	$Si_{0.3}S_{0.5}Sn_{0.2}$	45	0	1.08	0.61	-0.68	5.0	823
3	$Si_{0.3}S_{0.5}Ge_{0.2}$	44	0	1.26	0.56	-0.57	5.0	871
4	$S_{0.3}Ge_{0.1}Sn_{0.6}$	37	0	1.12	0.54	-0.62	5.0	662
5	$Si_{0.3}S_{0.7}Te_{0.3}$	34	0	1.17	0.45	-0.37	5.2	728
6	$P_{0.1}S_{0.4}Ge_{0.5}$	32	0	1.14	0.58	-0.38	4.9	734
7	$Si_{0.2}Se_{0.2}Sn_{0.3}$	32	0	1.19	0.59	-0.67	5.0	768
8	$Si_{0.3}S_{0.4}Te_{0.2}$	31	0	1.27	0.48	-0.53	5.2	784
9	$Si_{0.3}S_{0.4}Te_{0.1}$	26	0	1.14	0.60	-0.52	5.0	868
10	$P_{0.1}S_{0.4}Ge_{0.3}$	26	0	1.11	0.60	-0.40	5.1	698
11	$Si_{0.4}P_{0.2}Se_{0.3}$	20	0	1.05	0.46	-0.34	4.9	913

Fig. 22 Screening environment-friendly OTS materials. **a** The first screening filter of element exclusion for new OTS materials. **b** The screened compositions for the valence electrons number per atom N_{ve}, the glass-transition temperature (T_g) and the 5 valence-electron rule. **c** Mobility gap E_μ and trap gap ΔE_t. **d** Formation energy E_{form} and trap gap ΔE_t. **e** Element breakdown of screened compositions. **f** Summary of 11 promising OTS compositions of selector materials [98]. Adapted with permission from [98]. Copyright 2022, IEEE

behavior (Fig. 22b). For the about 1500 compositions that passed the above screening, they computed the formation energies and the electronic properties from first-principles. After considering formation energy < 0 eV atom^{-1} (chemical stability), low leakage current, immunity to phase demixing, application-specific trap/mobility gaps and change in polarizability, they finally identified 11 promising OTS materials (Fig. 22f), including $P_{0.2}S_{0.4}Ge_{0.4}$, $Si_{0.3}S_{0.5}Sn_{0.2}$, $Si_{0.3}S_{0.5}Ge_{0.2}$ etc. Clearly, all these candidates were S-based compounds, indicating the application potential of S-based OTS materials [98, 99].

Different from the above computational screening, Wu et al. performed a systematic materials screening of chalcogenides from the periodical table of elements using three essential criteria—few elements (easy fabrication), wide mobility gap (low I_{off}), and thermal stability > 400 °C (withstand BEOL process) [100]. The anions were S, Se, or Te, while cations of these chalcogenides were from group III to V located at metal–semiconductor boundary (Fig. 23a), which were widely used in phase change materials. After the above three essential criteria filtering, Ga–S was selected as the final research target due to its high mobility gap of ~ 2.53 eV and high crystallization temperature of ~ 550 °C (Fig. 23b). Photothermal deflection spectroscopy experiment detected high-density traps in GaS materials required for OTS behavior (Fig. 23c). Further device results confirmed that Ga–S-based devices exhibited typical OTS switching behaviors, with a high drive current density J_{on} of ~ 21.23 MA cm^{-2}, a low I_{off} of ~ 10 nA, and a V_{th} of ~ 2.5 V (Fig. 23d-f).

Table 4 summarizes the device performances of S-based OTS selectors. As expected, S-based OTS selectors present large a J_{on} ranging from 5 MA cm^{-2} to 34 MA cm^{-2}, an I_{off} ranging from 10^{-8} A to 10^{-9} A, a V_{th} ranging from 2 V to 5 V, and an endurance > 10^8 cycles. A high thermal stability of > 350 °C and even 600 °C was also obtained. Clearly, Se-, Te-, and S-based OTS materials have their own advantages and limitations. The actual optimization process involves integrating these advantages and overcoming their shortcomings. This is why many OTS materials are combinations of these three sub-systems. Indeed, multi-component OTS materials have many performance advantages, but the increasing complexity of their compositions also brings numerous challenges. The complex multi-component systems make it difficult to achieve atomic-level compositional uniformity in OTS material thin films, and precise control of element ratios is also challenging. Consequently, complex multi-component systems are not easily prepared using advanced conformal processes such as ALD, which hinders the application of these materials in high-density 3D vertical architecture.

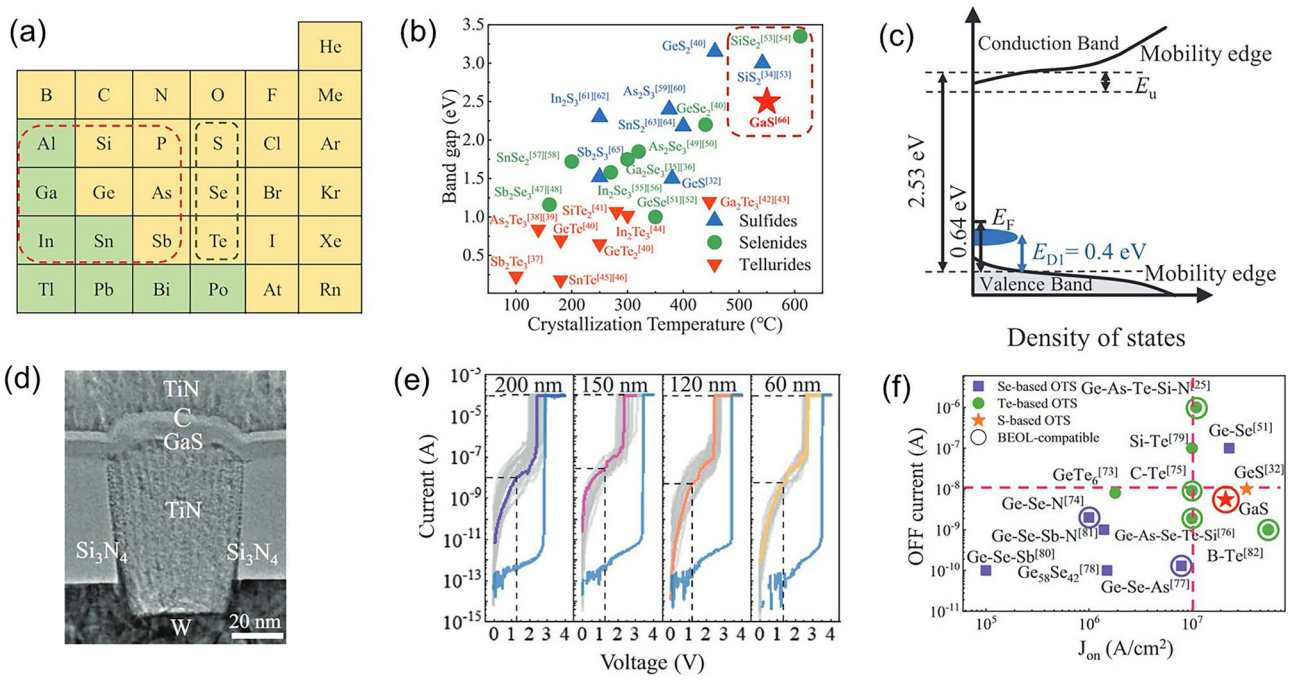

Fig. 23 GaS OTS selectors. **a** Pick out the cation and anion from the periodic table. **b** Band gap and crystallization temperature of these binary chalcogenides. **c** Experimentally reconstructed qualitative energy band schematic. **d** Device structure with 60-nm plug. **e** DC *I–V* curves. **f** Comparison of the I_{off} and J_{on} with other reported selectors [100]. Adapted with permission from [100]. Copyright 2022, John Wiley and Sons

Table 4 Performance summary and comparison of S-based OTS devices

Materials	Feature size/nm	Selectivity	J_{on}/MA cm^{-2}	I_{off}/A	V_{th}/V	V_{hold}/V	Speed/ns	Endurance	Thermal stability/°C
GeS [66]	190	10^6	34	10^{-8}	~3.2	~1.5	10	10^8	> 350
GeS [95]	60	10^5	35.4	10^{-8}	~2	~1.3	7	–	–
GeS [97]	60	10^4	3.54	2×10^{-8}	3.4	–	10–20	10^9	> 600
Ge_2S_3 [97]	60	10^5	3.54	$\sim1\times10^{-8}$	4	–	12–20	10^9	> 600
GeS_2 [97]	60	10^6	3.54	1×10^{-9}	5	–	15–20	10^9	> 600
Ge_2S_3(PE-ALD) [94]	50	10^4	~5	4.5×10^{-8}	4	–	–	–	> 600
GeS_2 (PE-ALD) [94]	50	10^4	~5	2×10^{-8}	5	–	–	–	> 600
Ge–S–As [96]	60	10^4	12	$<10^{-8}$	~2	~1.5	10	$\sim10^{10}$	> 450
Ga–S [100]	60	10^4	21.23	10^{-8}	~2	~1.5	–	–	~500

4 Switching Mechanisms of OTS

4.1 OTS Models

Since the discovery of OTS materials, many models were developed to explain the threshold switching phenomenon [16, 29, 101–110]. For instance, Kroll et al. proposed a *thermal runaway model* [103, 104] that explains the OTS as the result of a Joule heating process, which triggers a positive feedback loop for carrier generation and leads to an exponential increase of the conductivity. Nevertheless, the thermal model could not capture one of the most relevant feature of OTS: negative differential resistance (NDR) [111, 112]. While the thermal models were successfully applied to describe the NDR in single-crystal Si-doped YIG [113], in crystalline, large-gap semiconductors the

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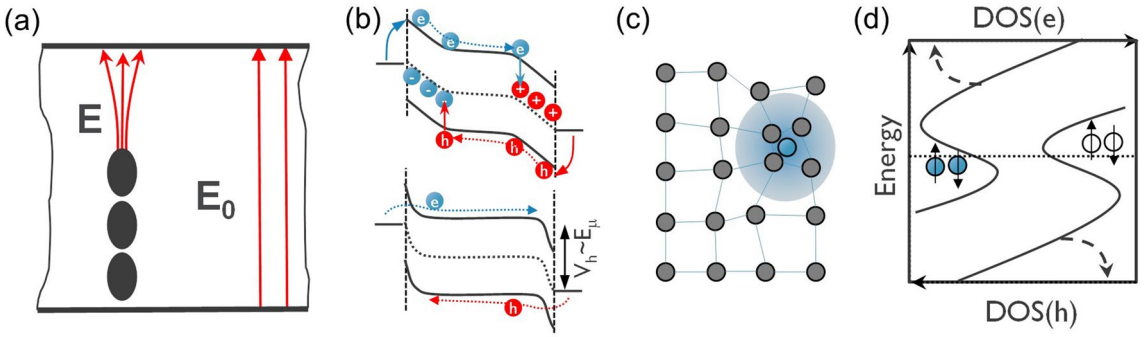

Fig. 24 **a** Field-induced nucleation model—the nucleation of conductive crystallite is in a highly resistive amorphous matrix that concentrates the electric field and drives the filament growth until the device is being shunted. Adapted with permission from [107]. Copyright 2007, AIP Publishing. **b** Carrier injection model—*e/h* free carriers are injected on both sides, neutralizing VAPs, which do not interfere anymore with the electronic transport. Holding voltage corresponds to the mobility gap energy. Adapted with permission from [115]. Copyright 1973, IEEE. **c** Small polaron model—trapped charge carriers modify the local atomic bonding environment. This bond rearrangement modifies the local morphology of the materials and reduces the carrier mobility considerably. Above a critical quasi-particle density, the destructive interference of the atomic displacements does not hamper the carrier transport any longer. **d** Density of States (DOS) for the 2-electron and 2-hole vs. their one-particle energies in amorphous matrix, where rare, special, local negative-U centers showing strong polaron effects provide its Fermi level pinning. Adapted with permission from [110]. Copyright 2012, AIP Publishing

NDR is not the result of an ovonic threshold switch. By the early 1980s, the thermal model was overthrown by the electric-field-driven OTS models [101, 114] that will be discussed below.

In PCM materials, OTS is the precursor mechanism of the ON switching that induces a local Joule heating process and the eventual crystallization of the amorphous into a high-resistance state phase. In this framework, Karpov et al. [105–107] introduced a *field-induced nucleation model* that assumes that the crystalline growth section, described as being a conductive cylinder in Fig. 24a, proceeds only once past a critical nucleus size of the filament. If the nucleus size is smaller than the critical size, the crystal seeds revert back into their amorphous phase upon field removal. This model is able to describe the drift dynamics of the threshold voltage upon device operation, highlighting the need to consider the amorphous matrix relaxation when dealing with drift dynamics. Its disadvantage is that it is not directly linked to the electronic properties of the material and hence does not properly account for its conductivity [23]. However, if one makes abstraction of the conductive cylinder/crystal grain/rod as to regard it as a (meta) stable (Ohmic) conductive local atomic percolation path, it contains an important ingredient for the universal OTS model; namely the bi/metastable state of the amorphous matrix and its associated relaxation time that defines the material parameter drift dynamics.

On the other hand, electronic switching models [102, 115–120] have been proved to be the most successful in describing the OTS conductivity and hence their associated threshold switching. In those models, the atomic bonding relaxation is not explicitly considered. However, many models consider the electron–phonon interactions or polaron relaxation implicitly. For instance, Ovshinsky [16] originally proposed an electronic mechanism at the origin of the threshold switching. The conduction was supposed to be phonon-assisted hopping near the Fermi level and not due to excited carrier conduction in the bands. The *carrier injection model* [115, 116] describes the conduction to be initiated when electrons and holes injected from cathode/anode compensate the positive/negative valence-alternation pairs (VAP) [101, 121–123] throughout the layer. The injected free carriers are transported in the mobility edges of the density of states. The holding voltage, therefore, reflects the mobility gap of the material (Fig. 24b), a correlation which was actually observed in a set of nine OTS materials [124]. Adler et al. [101] interpreted the threshold switching as originating from an impact ionization (II) process and formally described the NDR as being a competition between a carrier generation process (driven by both electric field and carrier densities) and a Shockley–Hall–Read (SHR) recombination. The model takes into consideration the electronic structure of the amorphous materials and together with the VAP theory [121], gives a detailed interpretation of

the changes that (might) occur at the atomic/electronic level. It is worth noting that the model considers a local bond rearrangement/coordination change that takes place upon charge trapping on defects, which is a short-range (intimate valence–alternation pair) mechanism and does not require any atomic drift or diffusion when the material switches on or off. In other words, the impact of atomic relaxation upon defect charging was only implicitly hinted. Redaelli et al. [102, 117] improved this description by adding an avalanche-like multiplication phenomenon to the list of carrier-generation mechanisms.

Emin's [125] *small polaron model* of subthreshold conduction was motivated by small measured Hall mobilities. From that perspective, the switching corresponds to the moment when the density of small polarons increases sufficiently to reach a steady-state threshold, namely when adjacent polarons show destructive interference and cancel-out the atomic displacements of other polarons (Fig. 24c), which breaks the carrier-phonon interaction. This model was challenged by high quality Hall measurements [126]. Also, since in the amorphous matrix the strong small-polaron interactions can occur at rare, special and local bonding arrangements [110], the polaron-like band transport is prohibited. Nevertheless, the model highlights the role of local atomic relaxations that impact on the electronic conduction and therefore on the OTS mechanism. For instance, the 2 electron-2 hole "intimate pairs" will pin the Fermi level (Fig. 24d) and the switching on can be successfully described by soft atomic potentials that exhibit the double-well potential signature with two states [110, 127].

Ielmini et al. [118, 119] introduced a *high-field Poole–Frenkel (PF) transport threshold switching model*, where the traps are located deep in the mobility gap (Fig. 25a) and trigger the switching of the I_{on} current at a certain non-equilibrium occupation of higher-energy traps. This results in a substantial nonuniformity of the electric field in the amorphous matrix. The model includes the implicit relaxation of the atomic matrix, irrespective of its physical origins (polaron relaxation or thermal vibrational contributions) to the trap energy through thermally-assisted hopping or tunneling mechanisms. The capacity of this model to describe the complete current–voltage signature contributed to its popularity.

A revisited version of the impact ionization and PF models was recently introduced by Fantini et al. [120] in a *bipolar avalanche model*, which describes the conduction as PF by majority holes at low electric field. These evolve into bipolar avalanche multiplication and ultimately the threshold switching is being triggered by this electron–hole cooperation, leading to a larger electron mobility compared to the hole one (Fig. 25b).

Buscemi et al. [108] introduced a *hydrodynamic-trap-assisted-tunneling (TAT) model* that considers the occurrence of temporary and progressive localization-delocalization of the states, creating conductive channels inside the insulating matrix. The transition rates are increased upon

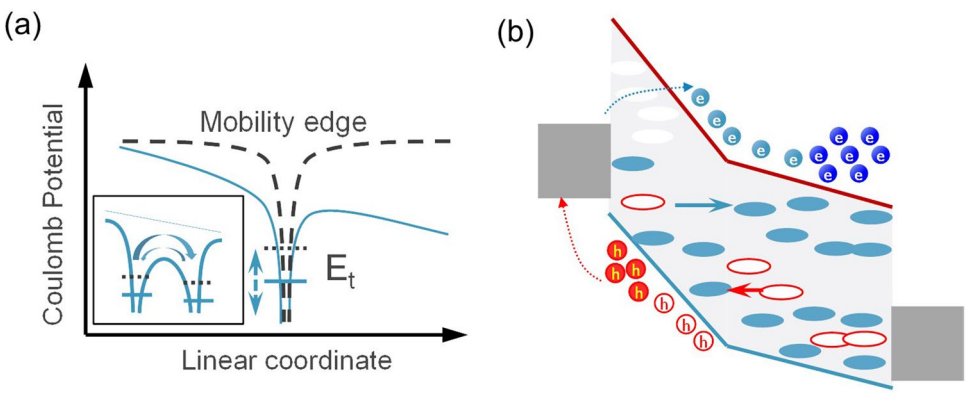

Fig. 25 **a** Poole–Frenkel model capture-emission depends on the trap energy depth (relative to the mobility edges) and density (inset: denser traps interact and the emission barrier reduced not only by the field, but also by the trap proximity), local phonon-related relaxation energy (vertical dashed arrow) can also be accounted for. Emission time is exponential on the trap depth; therefore, the effective carrier mobility increases in the direction of the electric field. This simple model takes the average trap properties. Adapted with permission from [119]. Copyright 2008, American Physical Society. **b** At threshold field, the carrier injection results in a nonuniform internal electric field, higher at the cathode, non-equilibrium trap occupation, generation of secondary electrons with high mobility and the OTS can be sustained afterward, even at lower fields. Adapted with permission from [120]. Copyright 2023, John Wiley and Sons

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the switching voltage as function of the excess energy from the hydrodynamic-TAT model solution. Aside from unclear atomic-electronic interaction mechanisms, the last two models are capable to reproduce most (if not all) experimental measurements of the OTS devices.

Degraeve et al. [127] used a *two-state model* with a double-well potential to describe the metastable percolation path/cluster/channel in the threshold switching. This approach makes abstraction of the exact details of the physical mechanism, but allows for a completely analytical solution for any arbitrary defect cluster. Thus, the model is capable of capturing technologically important phenomena like cycle-to-cycle and device-to-device variations within an acceptable computation time. Apart from electronic effects, the two-state model also considers self-heating. In particular, the switch-off is identified as temperature-controlled.

In the following, first-principles evidences are provided to unravel the nature of electronic properties and the nature of mobility gap traps in amorphous OTS chalcogenide materials. Their interaction with the electric field is discussed and the accompanying polaron relaxation mechanism that occurs upon charge redistribution in the amorphous systems. Finally, a discussion on the most plausible OTS mechanisms is given.

4.2 Electronic Structure of Disordered Materials

In analogy to crystalline semiconducting materials, the electronic structure of glassy/amorphous semiconducting materials can be described by a gap between the valence and conduction (mobility) edges (in contrast to bands in crystals), with additional tail and/or gap states in-between that are localized in space. These gap/tail states can act as electron or hole traps (or defects) [128]. Traditionally, the electronic structure and possible transport mechanisms are discussed in terms of these electronic structure defects. Kastner et al. [121] introduced labels for the under-coordinated C_1^- and over-coordinated C_3^+ chalcogenide atoms to represent the defect states that accepted/donated charges, calling them valence-alternation pair (VAP). In the same framework, over-/under-coordination can be extended to the elements of the group V (pnictogens $2P_3 = P_4^+ + P_2^-$) and IV (tetragons $2T_4 = T_5^+ + T_3^-$) [129–131] of the periodic table. The length of the trap localization is of the order of 1.5–2 nm [131]. This implies that atomistic models must meet a minimum size requirement. Typically, for density-functional-theory (DFT) simulations to be affordable, a model size of ~ 2 nm results in a trap concentration of ~ 10^{21} cm^{-3}. This is a rather large concentration, compared to ranges measured of 10^{18}–10^{19} cm^{-3}. Despite this artificially high trap concentration, DFT simulations provide a glimpse at the electronic signature of the chalcogenide materials. Investigating various compositions of Ge_xSe_y, with x:y = [50/50 Ge-rich, 30/70 Se-rich], Clima et al. [129, 130] observed over-coordinated Ge_5^+ (electronic traps) and under-coordinated Ge_3^- (hole traps) VAP states or Se non-bonding lone pairs (LP) (hole traps) localized states in Se-rich compositions (Fig. 26a), whereas in Ge-rich models there were mostly Ge–Ge chains of atoms, playing the role of electron/hole

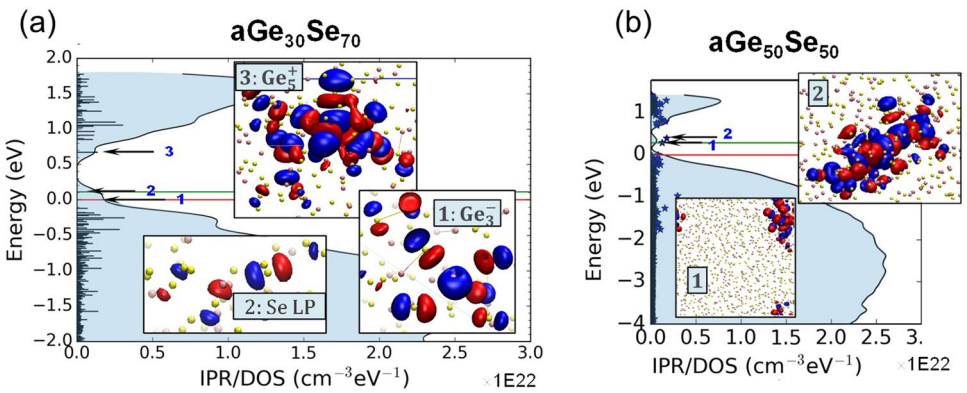

Fig. 26 **a** Typical DOS in 2 × 2 × 2 nm Se-rich $aGe_{30}Se_{70}$ model with few Se-LP, Ge_3^-/Ge_5^+ VAP gap/tail states representations as insets. **b** Typical DOS in 3 × 3 × 3 nm Ge-rich $aGe_{50}Se_{50}$ model with few representations of gap/tail states. The red line denotes the Fermi level, the green line-the first empty state. The Se lone pairs and non-tetrahedral/co-linear bonds around Ge are typical for the mobility gap traps. Adapted with permission from [129]. Copyright 2020, John Wiley and Sons

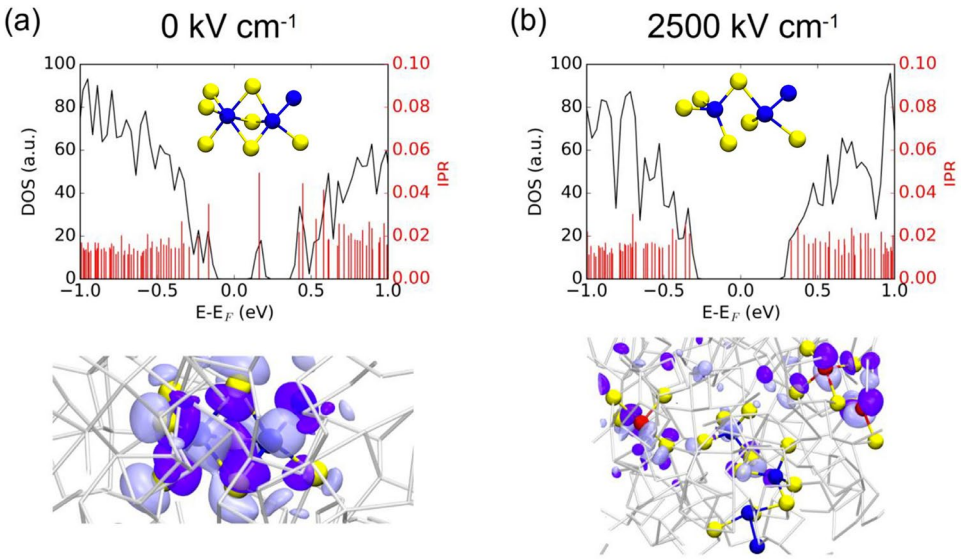

Fig. 27 Density of States (DOS), Inverse Participation Ratio (IPR-degree of localization) and local atomic coordination for the **a** localized mid-gap state in the absence of electric field and **b** under 2500 kV/cm field. Adapted with permission from [134]. Copyright 2022, Elsevier

traps (Fig. 26b). It was shown that even within the fixed-atoms approximation, the electric field has a strong influence on the energy and localization length of the tail states.

An applied electric field can promote electrons to higher energy states. If the higher-energy states are of antibonding character, the local bonding will be weakened and become unstable after this electronic excitation. The probability of encountering an electron promotion to the antibonding state is high in amorphous chalcogenides that have on average five valence electrons per atom (the 5 valence-electron rule [132, 133]). Konstantinou et al. [134] elaborated in details on the effect of the electric field on the mid-gap states in amorphous $Ge_2Sb_2Te_5$ chalcogenide. It has been shown (Fig. 27) that 1–2.5 MV cm^{-1} applied electric fields are capable to break/reconnect and change the local coordination around the atoms hosting the localized mid-gap electronic state. This removes the trap from the mid-gap by transforming it into a delocalized conduction-edge state. This local instability is key in activating the OTS mechanism, which reflects the transition from insulating to conducting state of the material [135–137]. The work clearly shows that considering the effect of the electric field on the electronic structure defect in the gap (inherently linked to the local bonding/coordination) is required, when describing the OTS mechanism.

4.3 Polaron Relaxation

At this level, it is interesting to understand what happens to the gap defect levels when they are getting populated. An important thing to describe the charge transport mechanism is to consider the atomic relaxation that inherently occurs during trap (de)occupation process. Nardone et al. [110] gave an elegant description of the strong interaction between the charged carriers and local atomic bonding in chalcogenide glasses. They argue that a high DOS in the mobility gap indicates that localized states in the mobility gap could provide with sufficient screening of the external field by forming a dipole layer by means of a redistribution of localized electrons [110]. This redistribution is accompanied by a set of local atomic deformations, similar to the lattice polaron relaxation but spatially localized in the amorphous matrix. In terms of atomic bonding, it can be pictured as if certain weakly bonding atomic morphologies are forming small “liquid-like” regions that got “frozen” in the solidified glass. In another context, these regions are known under the name of excitation lines or space–time bubbles [138]. Experimental evidences are pointing to the negative correlation (Hubbard/U [122]) energy nature of the amorphous chalcogenides. In other words, these doubly-occupied localized states are stabilized energetically by a polaron relaxation mechanism and single occupation exists

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only as excited states. These are supported by the lack of ESR signal at non-cryogenic temperatures. The Fermi level pinning with an activation energy for the conduction that is half the mobility gap supports the view that a strong polaron interaction is characteristic to the chalcogenide glasses that sets them apart from other amorphous semiconductors [110]. All these factors favor the 2e/2 h excitation model for the polaron conduction, that can well be described by a two-state model with conduction through a percolation channel [127].

Although unequivocally proving that the strong polaron interaction is responsible for electronic transport is challenging, we want to highlight in the following the importance of local structural relaxations upon trap charging by giving a few supporting theoretical findings. Raty et al. [137] studied with first-principles electronic excitations of the OTS glasses. Their results showed structural reordering, bond alignment, and appearance of local structural motifs that are characteristic of meta-valent bonds [138–140]. Next, the Born effective charges (BEC) of certain atoms increase drastically upon electronic excitation. These changes lead to large DOS/dielectric constant changes, hence reflecting a modulation of the conductivity of the material [141]. Noé et al. [136] argue that the bond alignment/delocalization is expected to introduce more conductive channels at the Fermi level of the amorphous OTS materials. Based on a BEC increasing upon trap charging, an OTS-gauge factor was defined to assess the material's ability to undergo a threshold switch for theoretical screening purposes [98]. Another illustration of the impact of the polaron relaxation model in amorphous $Ge_{50}Se_{50}$ was given by Slassi et al. [142] whose results stressed the dramatic changes in the mobility gap undertaken by the amorphous matrix.

These models illustrate that atomic relaxation mechanisms are driving part of the electronic structure change taking place during the threshold switching process. That, together with the thermal Joule heating effects during switching or longer time operation of the device, leads to bond readjustments and therefore to a relaxation of the amorphous matrix with an eventual resistance/threshold voltage drift [105, 129, 143].

4.4 Conduction-Switching Mechanisms Discussion

Off-state conduction: Nardone et al. [110] analyzed various conduction mechanisms in amorphous chalcogenides. They identified, in combination with experimental data, the most plausible electronic conduction mechanisms, namely: Poole–Frenkel ionization [118–120], field-induced delocalization of tail states, optimum channel hopping in thin films, optimum channel field emission, percolation band conduction [127], or transport through crystalline inclusions. The latter might be relevant for PCM materials, but it can safely be excluded for non-crystallizing OTS materials. Next, space-charge limited currents are only plausible in thick films and low temperatures conditions, whereas Schottky emission and classical hopping conduction (tunneling from trap to trap) were deemed very unlikely to occur. Finally, the multi-phonon trap-assisted tunneling (TAT) [108] was successfully used in describing the off conductivity.

Switching: electronic models describe the switching process as being a non-equilibrium condition for the trap occupation that alter the electronic structure [101, 102, 115–120]. A more physical description of the threshold switching mechanism requires considering both electronic and ionic dynamics events: when the mobility gap defects/traps get populated, a local atomic bond alignment/rearrangement (polaron relaxation) leads to different trap position in energy and to a spatial (de)localization [110, 129, 131, 136, 137, 139, 144]. As a consequence, the charge transport properties change dramatically, but reversibly. Most OTS switching models describe the same phenomenon at different abstraction level using different frameworks. For instance, the small polaron model describes the onset of the conduction at the polaron density that leads to destructive interference of atomic bond deformations of nearby polarons, whereas in PF model, the same phenomenon can be described by energy-aligned close in space traps with small hopping barrier that would effectively transform the traps into a delocalized subband. Also, the phonon-assisted hydrodynamic-TAT model considers the local polaron relaxation with the energetic load-relaxation of the traps upon charging, whereas the two-state model accounts for it with a double-well potential between localized and charged/relaxed/delocalized states. The level of description is a trade-off between physical precision and computing speed. Important practical phenomena like device-to-device variability can only be captured when abstraction of the atomistic mechanism is taken. Consequently, it is not straightforward to dismiss certain models over others since they are all mostly complementary to each other, if not the same on the grand scale. While one could argue that many aspects of the conductivity and switching

are accurately described mathematically by selecting one or combining several models (see, for instance, Fantini et al. [120] for the latest/ most comprehensible model on OTS switching), there is no definitive proof of the exact physical mechanism behind the phenomenon. It could also be that several different conduction mechanisms are active at different electric fields or in different materials. The exact atomic/ electronic physical mechanisms are still difficult to prove experimentally and claim a full understanding of.

On-state conduction: In terms of spatial distribution of the current, some models treat the conductivity to occur in confined space of the device (filamentary/percolation), while others consider the conduction to be bulk-limited [118, 119]. However, when the device size is reduced, the bulk mechanism can be applied successfully to the confined space as well. Percolation conduction (optimum channel hopping, (sub)band conduction in variable trap densities) is naturally suiting amorphous materials with a conductivity field dependence as that of the PF conductivity [110]. Next, concepts based on a band conduction at the (modified) mobility edge or an impact ionization/avalanche multiplication also describe well the *on*-state conductivity. Indeed, the *on* state is not stable in absence of a flowing electrical current; as a consequence, the trap occupation state and delocalization are determined by the trapping/de-trapping dynamics. Then the rate of incoming electrons to maintain an average-full state of all the traps in the material is not sufficient, the atomic configuration around the trapping sites relaxes, leading to a charge localization and breaking the conductive cluster/ percolation path/channel.

To summarize, in the subthreshold regime there is a trap-limited current that can be described by more than a single plausible physical mechanism. Electric field and charge injections affect not only the occupation, but also the localization in space and in energy of the gap traps. At threshold switching, a non-equilibrium trap occupation (possibly also delocalization) occurs, which leads to a metastable state of the (cluster of) traps that conduct the carriers leading to either a (sub)band charge transport and/or also to an impact ionization/avalanche multiplication. A mix of both electronic and hole types of conductivities is likely to take place. The metastable state of the traps is retained by the electrical current until it is not sufficient to maintain them in the high-energy state (charged state), since the de-trapping rate is out of equilibrium with the trapping one and the system reverses back to the initial state (uncharged traps). Thermal effects on atomic relaxation are important ingredients in changing the conductive properties of the percolation path in the OTS material, which define the long-term evolution of the conductive path (aging, endurance, parameter drift).

5 Applications of OTS

When OTS devices were initially proposed in 1960s, their primary application purpose was to serve as a new type of rectifier device, aiming to replace conventional diodes [20, 20, 101]. However, due to challenges related to material and fabrication compatibility, OTS selectors did not gain significant advantages over diodes in the early stages of development. The latter, together with MOSFET, dominated the electrical semiconductor in the latter half of the twentieth century. Entering the twenty-first century, as the semiconductor process node advanced, conventional diode and MOSFET-based memory technology, that is, DRAM and Flash, nearly approached the physical limit, high-density emerging memories thereby were highly desired. The OTS device, as a promising selector unit in high-density arrays, regained wide research attention and ultimately achieved successful industrial applications in 2017 [11]. Besides being a switching selector, the recently reported OTS-only self-selecting memory in 2021 is a milestone for the OTS device, aiming to achieve low-cost and high-density memory [145]. Moreover, with the rise of the concepts such as neuromorphic computing and artificial intelligence (AI), there is an increasing interest in exploring the hardware platforms and devices that serve as carriers for computational theories [146]. The OTS device, with their excellent device consistency and superior scalability, also holds significant value in the field of neuromorphic computing. In this section, these potential applications of the OTS device are discussed in detail.

5.1 3D Memory

With the deepening research on next-generation fast-speed and high-density memories, the application of OTS in 3D novel memory, particularly in 3D PCM, has gradually become one of the major directions for OTS devices. The remarkable advantage of OTS, with substrate-free two-terminal structure, lies in its extremely high area utilization. Compared to MOSFET ($> 8F^2$) and bipolar switches ($5F^2$),

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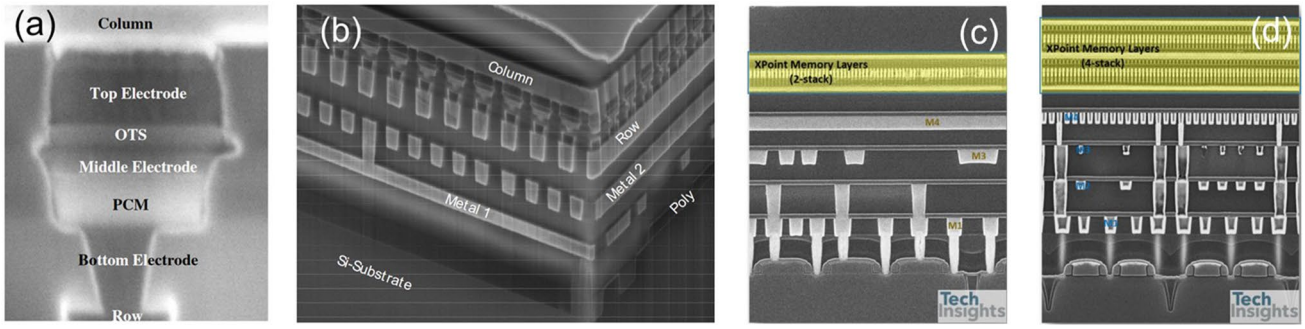

Fig. 28 1S1R structure in PCM. **a** Vertically integrated memory cell of 1S1R. **b** One layer of the PCM array fully integrated with CMOS [11, 12]. Adapted with permission from [11, 12]. Copyright 2009/2020, IEEE. **c** First-generation 2-deck 3D Xpoint array. **d** Second-generation 3D XPoint with 4-deck array [147]

the combination of OTS and PCM in a 1S1R configuration can achieve $4F^2$, which is a critical requirement for 3D high-density stacking-a key aspect of miniaturization. Over the past 20 years, PCM technology not only underwent aggressively size scaling from 180 nm to 20 nm, but also experienced a revolutionary evolution of the selector cell from the initial silicon-based MOSFET and bipolar junction transistor (BJT) to the OTS technology, successfully enabling the increasing capacity from 4 Mb to 256 Gb [11, 12, 25–28].

In 2009, Intel's research team first reported the 1S1R 3D stacking technology [11] (Fig. 28a, b). In August 2015, Intel and Micron jointly announced the 3D Xpoint chip based on "bulk change" technology (a novel PCM device structure). In 2017, Intel introduced the Optane series chips based on 3D PCM technology to the market, including Optane solid-state drives (SSD) for the enterprise market and Optane flash memory for the consumer market. These chips were manufactured using mainstream 20-nm process technology, with a two-layer stacking. The optimized Ge–Se–As–Si OTS materials was believed to be used in the PCM-based Optane, achieving a storage density of 0.62 Gb mm^{-2} (Fig. 28c). This density was approximately 4.5 times higher than that of DRAM at the same 20-nm process node, with 91.4% of the core area occupied by the memory array [147]. In October 2019, Micron introduced the X100 NVMe enterprise SSD based on 3D PCM technology. Currently, 3D PCM with cross-point memory array has achieved four layers and 256 Gb per die in the second generation (Fig. 28d). The two generations of Intel's Optane memory, which are based on the 3D Xpoint structure, are the outstanding application of OTS devices. Although the next generation of Optane memory will not be introduced in the short term due to commercial and market reasons, the successful commercialization of the two generations of Optane memory serves as strong evidence for the application of OTS devices in memory technology.

Process complexity and cost are the main factors behind the current suspension of 3D Xpoint business. Moreover, as the number of stacking layers continues to increase, the cost per bit will significantly increase rather than decrease, due to the high dependence on lithography. The persistently high cost issue will be one of the challenges that the 3D Xpoint structure will inevitably face in future [148]. Therefore, the concept of using vertically integrated "true" 3D structures for high-density storage is gradually gaining attention. Although there is currently no fixed standard for vertical memory architecture, we can be certain that in vertical structures similar to 3D NAND, OTS materials will continue to play a role as the "select layer" integrated with the memory cell [149, 150]. Furthermore, the OTS device can be applied not only to PCM but also to other emerging memories, like resistance random access memory (RRAM), and still holds great application prospects in 3D storage technology.

5.2 Self-Selecting Memory

As aforementioned, the 3D Xpoint structure will face increasing manufacturing costs as the number of layer increase (Fig. 29a) [148]. This issue could potentially be addressed by adopting vertical architecture. However, it is foreseeable that for the current 1S1R structure, there are inherent process difficulties in precisely controlling the composition and ensuring atomic-level homogeneity in the film. In addition, the traditional 1S1R structure requires a

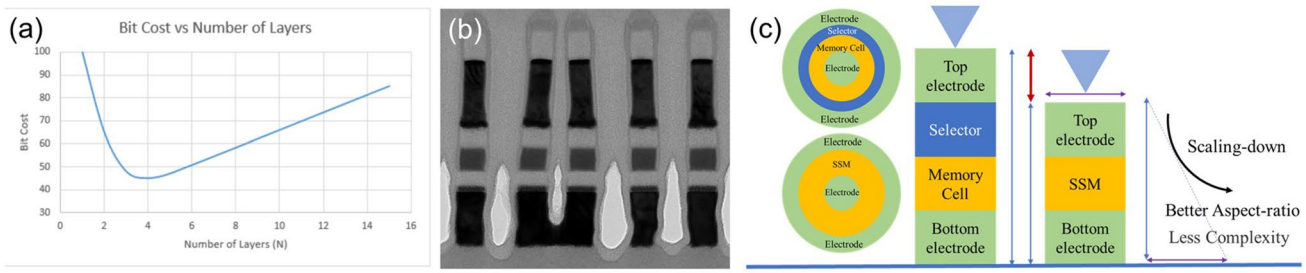

Fig. 29 **a** The bit cost versus number of layers [148]. **b** An example image of leaning and the resulting bridges in 3D XPoint structure. Adapted with permission from [151]. Copyright 2022, IEEE. **c** Concept of SSM (Self-Selecting Memory) in vertical and plane structure

memory cell to be connected in series with an independent selector, resulting in a small overall aspect ratio, which will bring about process problems such as "leaning" involving the overall strength of the device as the process node scales down (Fig. 29b) [55, 152, 153]. To address these issues, a new technology path known as "self-selecting" has emerged, aiming to converge the selector and memory into a unit without the need for another separate device [154–157]. Memory devices based on this architecture are referred to as "self-selecting memory (SSM)" (Fig. 29c). This concept goes beyond the self-select of the memory cell in 0T1R structure and includes the implicit concept of self-memory in the 1T0S structure. To realize this technological concept, the measurable parameters used to represent the stored data must be designed to ensure the stability, repeatability, and a large enough difference between two (or more) states to enhance the data retention and maintain the access window.

The OTS selector, being typical volatile device, is impractical for storing data using the conventional binary *on/off* states. Interestingly, V_{th} in OTS selector were found to be influenced by many factors such as device structure variations, the amplitude of applied pulses [158], pulse width [159], ramp rate [160], and relaxation time [161]. Ravsher et al. in late 2021, observed the control of the V_{th} of OTS device (composed of Ge–Te–As–Si) by the polarity of the applied voltage, more specifically, a systematic and stable changed with the alterations in polarity of the applied voltage (Fig. 30) [145]. The value of V_{th} in the current operation was closely affected by the polarity of the previous pulse, resulting in the generation of two relatively stable V_{th} levels, V_{th1} and V_{th2}, within the same pulse direction. In this work, the negative polarity V_{th} difference ($\Delta V_{th} = |V_{th1} - V_{th2}|$) was 260 mV, while the external resistance increased, further enhancing the ΔV_{th} (Fig. 30c). Exploiting this stable ΔV_{th}, which could persist for at least 1000 s (~ 17 min) as reported, enabled the independent utilization of OTS device for binary storage device, called OTS-only SSM.

Subsequently, the research team reported on the optimized device in mid-2022 [162], focusing on their application in the 1S1R structure. The device employed Ge–Se–As–Si OTS material. The improved device exhibited a further increase in the ΔV_{th}, ~ 1 V, and the positive ΔV_{th} became more pronounced. The SSM, which was in series with a Ge–Sb–Te PCM cell (Fig. 31a), aimed to enhance the performance

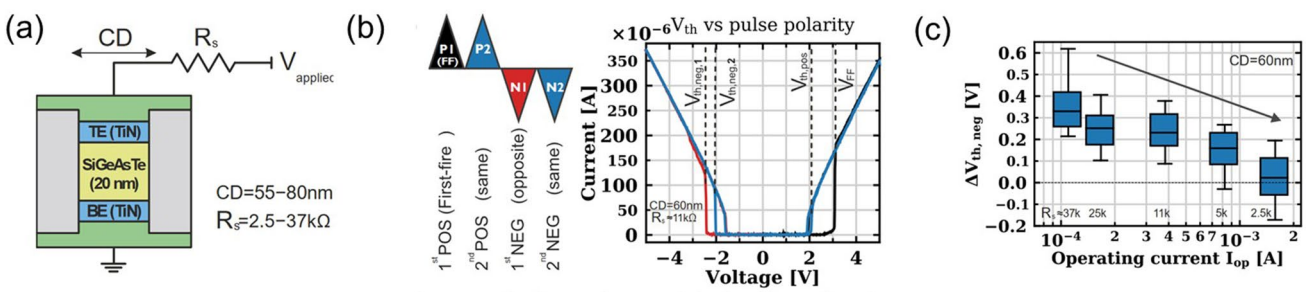

Fig. 30 Ge–Te–As–Si OTS-based SSM. **a** Device Structure. **b** *I–V* curves, indicating the polarity effect in OTS device. **c** Negative versus I_{op} with different resistance, the ΔV_{th} increased with the resistance rising [145]. Adapted with permission from [145]. Copyright 2021, IEEE

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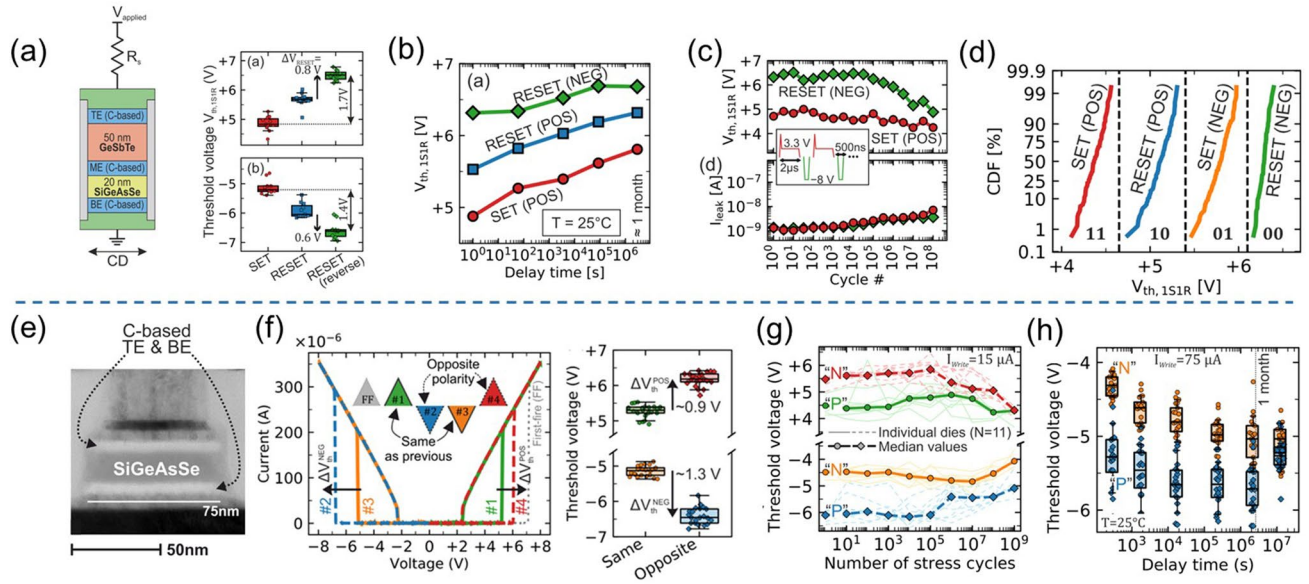

Fig. 31 Ge–Se–As–Si 1S1R cell and SSM. **a** Structure of the 1S1R cell and the distribution of its margin window. **b** > 1-month Retention. **c** Endurance over 10^8 cycles. **d** Four storage levels induced by the polarity effect. Adapted with permission from [162]. Copyright 2022, IEEE. **e** SSM with 75 nm feature size. **f** *I–V* curves and the distribution of negative and positive ΔV_{th} [162, 163]. **g** Endurance characteristics under bipolar stress. **h** Retention measurement. Adapted with permission from [163]. Copyright 2023, IEEE

of traditional 1S1R cell by offering double SET states and RESET states, each with a distinct difference. By employing voltage operation with different polarities, the originally small margin window (0.85 V) was effectively enlarged to ~ 1.7 and ~ 1.4 V. The 1S1R cell demonstrated a rather long retention reaching up to 1 month @ 25 °C (Fig. 31b) and an endurance over 10^8 cycles (Fig. 31c). Additionally, the significant difference among the four states indicated the potential for multi-level storage with four resistance states and even more (Fig. 31d). If the PCM itself has the potential to achieve multi-level storage, then the polarity operation of OTS devices may enable doubling of the storage states.

Recently, Ge–Se–As–Si-based SSM device with C-based electrodes was reported by the same research team [163]. The device exhibited a larger positive ΔV_{th} of ~ 0.9 V and negative ΔV_{th} of ~ 1.3 V (Fig. 31f), an ultralow writing current < 15 μA and a high endurance > 10^8 cycles (Fig. 31g). However, the SSM device showed some limitations in data retention. With a write operation performed at 75 μA, the window could be reliably maintained for 1 month @ 25 °C (Fig. 31h), and nearly disappeared after five months. If a lower operating current ~ 15 μA was employed, the data retention of the device further decreased to ~ 10 days, indicating that the SSM device cannot currently be considered a typical non-volatile memory without compositional and structural optimizations. However, it can be utilized as a "DRAM-like" memory with a longer refresh period, and the non-destructive "Read" operation can be used for refresh operation.

In 2022, Hong et al. [151] from SK Hynix fabricated a prototype of a 32 Mb SSM (Fig. 32a), strongly confirming the feasibility of engineering SSM for practical applications. The simplified device structure provided a larger aspect ratio, enabling it to maintain a good switching window even at the 15-nm process node (Fig. 32b). The device exhibited high endurance exceeding 10^7 cycles (Fig. 32c) and a rather low I_{op} (Fig. 32e). The unique structure of the SSM effectively suppressed the increasingly significant thermal disturbance in downscaled PCM (Fig. 32d). Through four generations of product iterations, the margin window of the prototype has slightly surpassed that of PCM in 3D Xpoint (Fig. 32f).

In summary, the innovative SSM technology offers a promising path for future application of the OTS device. Additionally, the endurance of OTS devices, resulting from their switching behavior, replaces the repetitive amorphous–crystalline phase transition in PCM, leading to significantly improve the endurance. Furthermore, the use of OTS device's threshold current/voltage instead of PCM's operating current/voltage

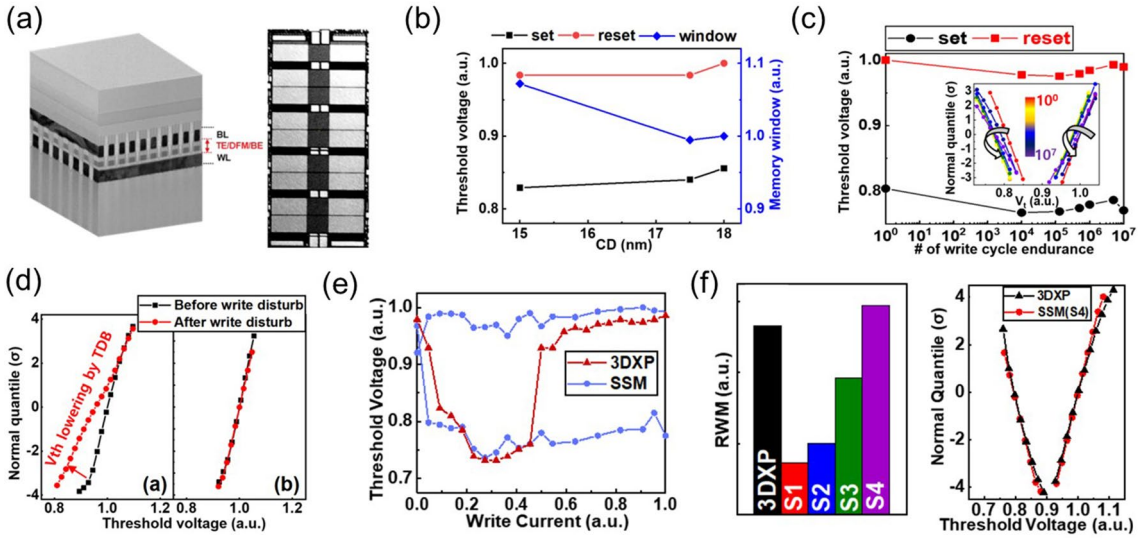

Fig. 32 SSM prototype. **a** Structure of the SSM array. **b** Variations of V_{th} and the memory window with the device scaling down. **c** Endurance and the distribution of V_{th}. **d** Distribution of V_{th} before and after the driven thermal disturbance. **e** V_{th}–I curves between 3D Xpoint and SSM. **f** Comparison of the margin window with 3D Xpoint [151]. Adapted with permission from [151]. Copyright 2022, IEEE

eliminates the need for melting the chalcogenide material, resulting in a notable reduction in energy consumption.

5.3 Neuromorphic Computing

In the traditional von Neumann architecture, which separates storage and computation, there is an inherent "memory wall" problem, which becomes more pronounced as the process node scales down [5, 164]. With the recent resurgence of AI technologies, a series of bio-inspired neural computing architectures have gathered significant attention due to their potential for achieving ultra-low power consumption and large-scale, highly parallel and high-speed computing. The neural computing platform and its devices, as the physical embodiments of these neural computing architectures, have naturally become a focal point of research. The physical realization of artificial neurons, synapses, and other bio-inspired devices is one of the key challenges in neuromorphic computing [165–172]. Mainstream novel computing architectures include spiking neural networks (SNNs), deep neural networks (DNNs), and in-memory computing. For a long time, the physical implementation of these computing architectures relied on combinations of CMOS and non-volatile memory (e.g., PCM, RRAM) [165–168, 173–175]. Early on, OTS played a role as a selector, primarily in combination with the memory, to suppress leakage currents, reduce power consumption, and restrain crosstalk, which is particularly crucial in large-scale arrays [146]. However, selector unit did not directly serve as artificial neurons and synapses themselves at that time.

The spiking neural networks exhibit remarkable potential in reducing the computational energy consumption due to their event-based and data-driven nature. However, the lack of a general learning rule hampers their ability to construct the large-scale networks. Recent reports suggest that SNNs can be constructed by transforming pre-trained artificial neural networks (ANNs). In this transformation, the neuron units are simplified to integrate and fire (I&F) neurons, which integrate input synaptic current and charge the membrane potential [176–179]. Once the membrane potential reaches the threshold voltage, the neuron generates spikes to the next synapse layer and resets the membrane potential. This characteristic aligns well with threshold switching devices [169], as traditional CMOS-based neurons suffer from large size and high power consumption [180–183].

Hence, the selectors, including NbO_2-based MIT devices, B–Te-based OTS devices, and Ag/HfO_2-based ionic-diffusion devices, have been investigated by Lee et al. as potential components for I&F neurons [184]. The study revealed that the B–Te OTS device exhibited excellent comprehensive performance, showcasing a low I_{off} of ~ 5 nA (Fig. 33d) and a short switching time of < 10 μs. These features contribute

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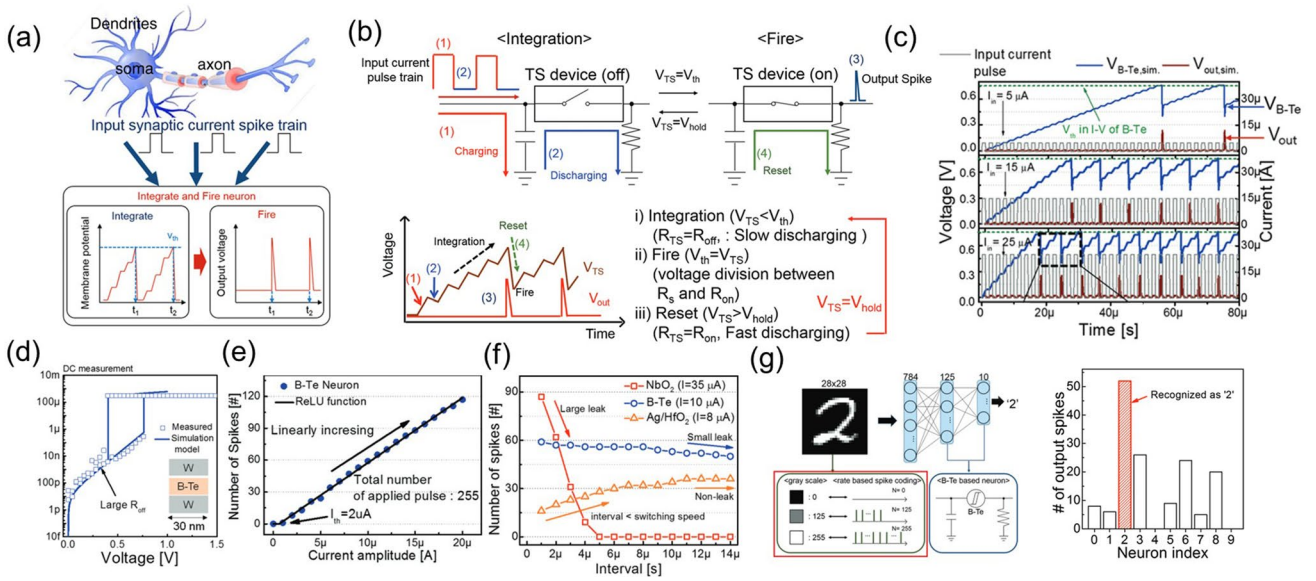

Fig. 33 Integrate and fire (I&F) neuron based on B–Te. **a** Concept of integrate and fire (I&F) neuron. **b** Schematic and Operation principle of I&F neuron. **c** *V–t* curves of neurons based on B–Te under different input current. **d** *I–V* curves of B-Te; **e** Number of spikes versus input current amplitude in B–Te selector, indicating the typical ReLU function. **f** Number of spikes as a function of pulse interval. **g** MNIST classification and the result of recognition [66, 184]. Adapted with permission from [184]. Copyright 2019, John Wiley and Sons

to improved leakage behavior and signal responsiveness in the operation of I&F neurons based on B–Te OTS devices. The relationship between the output pulse count and input current of the B–Te OTS device followed a typical rectified linear unit (ReLU) function (Fig. 33e). Additionally, the device demonstrated a higher operating bandwidth and more stable response characteristics in the relationship between output pulse count and input signal frequency tests (Fig. 33f). Remarkably, the B–Te OTS device also exhibited outstanding energy efficiency, with power consumption reducing to 30 pJ per spike. Subsequently, the research team employed I&F neurons based on B–Te OTS devices to process frequency-encoded ANN data in an SNN for handwritten recognition tests, achieving an acceptable recognition rate ~ 33% (Fig. 33g).

Lee et al. reported an artificial neuron device that consisted of an OTS selector and a few passive electrical components, capable of mimicking various behaviors of a biological neuron, including I&F, rate coding, short-term plasticity (STP), and chaotic activity [185]. They utilized a Ge–Se OTS device to construct an I&F neuron for testing, which exhibited favorable spike-frequency adaptation. Additionally, they documented the device's response characteristics in a chaotic system. The energy consumption per spike was estimated to be approximately 1.2 nJ per spike. Subsequently, by combining the OTS-based neuron device with reservoir computing techniques, they successfully performed spoken-digit recognition tasks with a significant level of accuracy ~ 94%.

The significance of sensing, memory, and computation integrated technology is increasingly evident [186–188]. In this domain, OTS device also found its potential applications. Lee et al. reported on the development of artificial sensory neurons based on a novel three-terminal OTS (3 T-OTS) [189]. The device utilized the Ge–Se–Ag system and allowed for V_{th} modulation through gate control. By integrating with a photodiode, they constructed an artificial retinal ganglion cell (RGC) (Fig. 34). This artificial RGC, combined with the reservoir-computing technique, was employed for classifying chest X-ray images into normal, viral pneumonia, and COVID-19 infections, achieving a recognition accuracy of approximately 86.5%.

In addition, random number generation is another vibrant application area, with significant importance in disciplines such as communication, computer simulation, and cryptography. Random numbers generated using the inherent stochastic properties of physical devices possess true unpredictability and non-repeatability [190, 191]. Hence, the

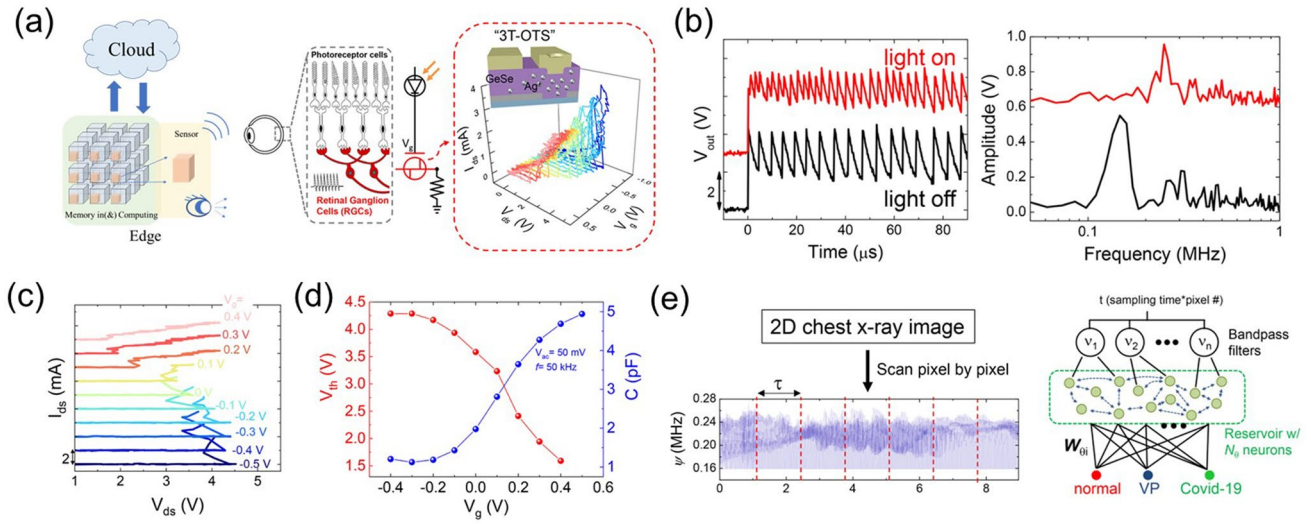

Fig. 34 3 T-OTS device as an artificial RGC. **a** Concept of edge- and cloud- computation, the diagram of RGC and an artificial RGC. **b** Response waveform of an artificial RGC with/without illumination, and the FFT spectra. **c** Variations of V_{th} under the modulation of V_g. **d** V_{th} and C versus V_g. **e** Classification of chest X-ray images between normal and other virus [189]. Adapted with permission from [189]. Copyright 2022, American Chemical Society

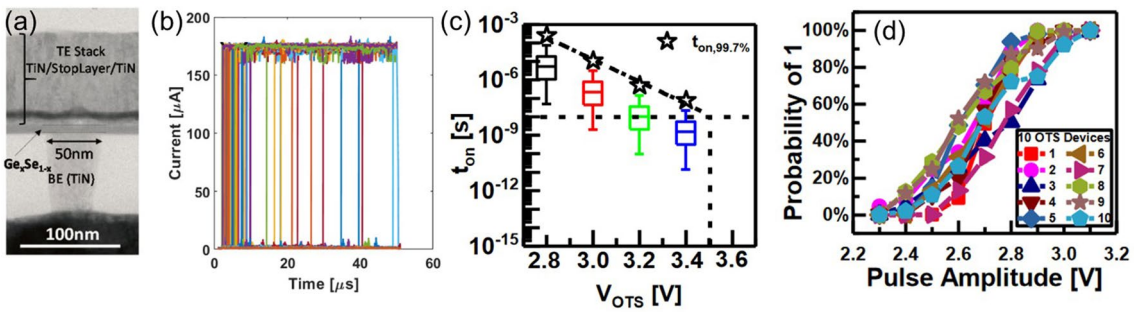

Fig. 35 Ge–Se-based true random number generator. **a** Device structure with 50-nm plug. **b** Distribution of $t_{delay\text{-}on}$ at 2.8 V. **c** Distribution of $t_{delay\text{-}on}$ at different biases. **d** Occurrence rate of "1" at different pulse amplitudes measured in 10 devices [196]. Adapted with permission from [196]. Copyright 2021, IEEE

development of true random number generators (TRNGs) based on device characteristics at the hardware level has become a prominent research focus [192–195]. Chai et al. conducted a study on TRNGs constructed using Ge–Se-based OTS device. The research revealed that the delay time (on/off) at a constant voltage follows the Weibull distribution (Fig. 35b), enabling the extraction and extrapolation of the switching probability dependence on pulse waveform, bias, and time (Fig. 35c). This feature facilitated parameter quantization and yielded highly random results. The generated 10^4-bit sequence successfully passed 12 tests in the NIST statistical test suite. Compared to RNGs composed of traditional non-volatile memories, the TRNG based on Ge–Se OTS devices exhibited a faster generation speed [196].

The volatile nature of OTS devices makes them well-suited for constructing non-weight storage elements in neuromorphic devices. Their typical switching behaviors have been predominantly utilized in the construction of ReLU functions for processing frequency-encoded data in current research. It should be noted that, at present, the training of weights often relies on preprocessing and input from external systems rather than being directly integrated within the OTS devices. While there are still

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many challenges to be addressed, OTS devices, with their favorable electrical performance and excellent scalability, hold promise for playing an important role in future neuromorphic computing.

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Declarations

Conflict of interest The authors declare no conflict of interests. They have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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