e-ISSN 2150-5551
CN 31-2103/TB

Nano-Micro Letters

ARTICLE

https://doi.org/10.1007/s40820-025-01674-8

Cite as
Nano-Micro Lett.
(2025) 17:154

Received: 31 October 2024
Accepted: 23 January 2025
© The Author(s) 2025

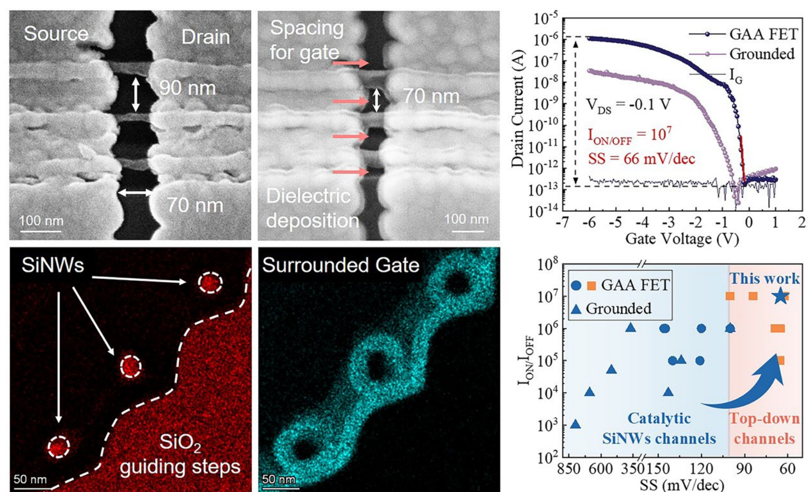
High-Performance Gate-All-Around Field Effect Transistors Based on Orderly Arrays of Catalytic Si Nanowire Channels

Wei Liao[1], Wentao Qian[1], Junyang An[1], Lei Liang[1], Zhiyan Hu[1], Junzhuan Wang[1], Linwei Yu[1] ✉

HIGHLIGHTS

- A high-density array of orderly silicon nanowires (SiNWs) was grown in precise locations, with diameter of $D_{NW} = 22.4 \pm 2.4$ nm and interwire spacing of 90 nm.
- A special suspension-contact protocol has been developed to reliably suspend the in-plane solid-liquid-solid SiNWs to serve as ultrathin quasi-1D channels for gate-all-around field-effect transistors (GAA-FETs).
- By optimizing the source/drain metal contacts, high-performance catalytical GAA-FETs have been successfully demonstrated, achieving a high on/off current ratio of 10^7 and a steep subthreshold swing of 66 mV dec^{-1}.

ABSTRACT Gate-all-around field-effect transistors (GAA-FETs) represent the leading-edge channel architecture for constructing state-of-the-art high-performance FETs. Despite the advantages offered by the GAA configuration, its application to catalytic silicon nanowire (SiNW) channels, known for facile low-temperature fabrication and high yield, has faced challenges primarily due to issues with precise positioning and alignment. In exploring this promising avenue, we employed an in-plane solid–liquid–solid (IPSLS) growth technique to batch-fabricate orderly arrays of ultrathin SiNWs, with diameters of $D_{NW} = 22.4 \pm 2.4$ nm and interwire spacing of 90 nm. An in situ channel-releasing technique has been developed to well preserve the geometry integrity of suspended SiNW arrays. By optimizing the source/drain contacts, high-performance GAA-FET devices have been successfully fabricated, based on these catalytic SiNW channels for the first time, yielding a high on/off current ratio of 10^7 and a steep subthreshold swing of 66 mV dec^{-1}, closing the performance gap between the catalytic SiNW-FETs and state-of-the-art GAA-FETs fabricated by using advanced top-down EBL and EUV lithography. These results indicate that catalytic IPSLS SiNWs can also serve as the ideal 1D channels for scalable fabrication of high-performance GAA-FETs, well suited for monolithic 3D integrations.



KEYWORDS In-plane solid-liquid-solid; Ultrathin silicon nanowires; Gate-all-around field-effect transistors (GAA-FETs)

✉ Linwei Yu, yulinwei@nju.edu.cn
[1] School of Electronic Science & Engineering, Nanjing University, Nanjing 210093, People's Republic of China

Published online: 19 February 2025

1 Introduction

Gate-all-around field-effect transistors (GAA-FETs, as depicted in Fig. 1a), which offer exceptional electrostatic control, are becoming the mainstream device architecture for technology nodes < N3 nm [1–4], where ultrathin crystalline silicon nanowires (c-SiNWs) are considered as ideal quasi-one-dimensional (1D) channel materials to mitigate the short-channel effect in highly integrated CMOS logics. However, to implement monolithic 3D integration that enables higher integration density, it is essential to fabricate ultrathin SiNW channels on the stacked layers, where a monocrystalline Si wafer substrate is absent. Instead of using a conventional top-down etching procedure in the bottom logic layer, these 1D SiNW channels should be grown in precise locations as orderly arrays directly on the insulating dielectric layer, via a low-temperature process to avoid thermal damage to the underlying logic layers [5–7].

To address this challenge, a low-temperature catalytic growth of such SiNW channels provides an ideal option, as it doesn't rely on the preexistence of c-Si wafer [8, 9]. Although the famous vapor–liquid-solid (VLS) growth mechanism has been widely exploited to produce high-quality SiNW channels for the demonstration of high-performance FETs and sensors [10–13], the vertical orientation of the VLS-grown SiNWs makes them difficult to integrate into the planar device architecture [14, 15]. Particularly, the post-growth transfer and release of individual VLS-SiNWs onto pre-defined electrode trench, for the subsequent formation of GAA-FET, lacks deterministic position and orientation control, and is thus technically incompatible with the standard planar manufacturing procedure [11, 16, 17]. In order to address this challenge, an in-plane solid–liquid-solid (IPSLS) mechanism [18–20] has been developed in our previous works, where indium (In) catalyst droplets absorb amorphous silicon (a-Si) precursor thin film to produce c-SiNWs along pre-defined guiding step edges. Indeed, a rather high-density integration of the IPSLS SiNWs has been demonstrated, under the guidance of terrace mini-steps [21, 22] or the sidewall grooves [23, 24], achieving an impressive diameter and uniformity control, backed by a series of tailored catalyst formation technologies [24, 25]. However, the performance of planar or GAA-FETs fabricated with catalytic SiNW channels still lags significantly behind that of state-of-the-art fin- or GAA gate FETs [11, 16, 17, 26]. Specifically, the subthreshold swing (SS) of the catalytic SiNW-FETs, a key indicator of the strength of electrostatic control, typically ranges from 850 to 100 mV dec^{-1} [27–33], which is still far from the theoretical limit of 60 mV dec^{-1}. For the IPSLS SiNWs, a genuine GAA-FET has not yet been demonstrated, and their potential to serve as 1D channels for high-performance FETs remains to be explored and verified through direct experimental evidence.

In this work, we focus on demonstrating the first-ever GAA-FET based on catalytic IPSLS SiNWs, by developing a series of critical channel-releasing and contacting techniques. First, ultrathin SiNWs with diameter of $D_{NW} = 22.4 \pm 2.4$ nm and interwire spacing of 90 nm were grown on a pre-designed sacrificial layer. Then, a specialized suspension-contact protocol was developed to reliably release these ultrathin channels, achieving suspended SiNWs with a maximal suspension length exceeding 500 nm. By optimizing the source/drain metal contacts, high-performance junctionless GAA-FETs have been successfully demonstrated, exhibiting an $I_{on/off}$ ratio of 10^7 and a sharp SS of 66 mV dec^{-1}. These results represent the first experimental evidence that catalytic grown SiNWs can also serve as high-quality channels for the fabrication of GAA-FETs, achieving high-performance comparable to those fabricated using sophisticated top-down EBL and EUV lithography methods.

2 Results and Discussion

The SiNWs were grown upon 500 nm oxide-coated c-Si wafer substrate, via IPSLS mechanism as depicted schematically in Fig. 1b. Specifically, the guiding terrace edges were first patterned by using lithography, followed by multiple alternating cycles of C_4F_8 and O_2 plasma etching processes in inductively coupled plasma (ICP) system, to form a multi-step guiding terraces, as specified in the Supporting Information. Subsequently, a 40-nm layer of Al_2O_3 was deposited as the sacrificial layer using atomic layer deposition (ALD). Then, as depicted schematically in the three panels of Fig. 1b, the IPSLS growth of SiNWs involves two major steps that is (1) the patterning and deposition of indium (In) catalyst stripes, of nominally 4 nm thick, at the starting ends of the guiding terraces. After loading into a PECVD system and being treated by H_2 plasma at 215 °C, the In stripes were transformed into discrete

© The authors https://doi.org/10.1007/s40820-025-01674-8

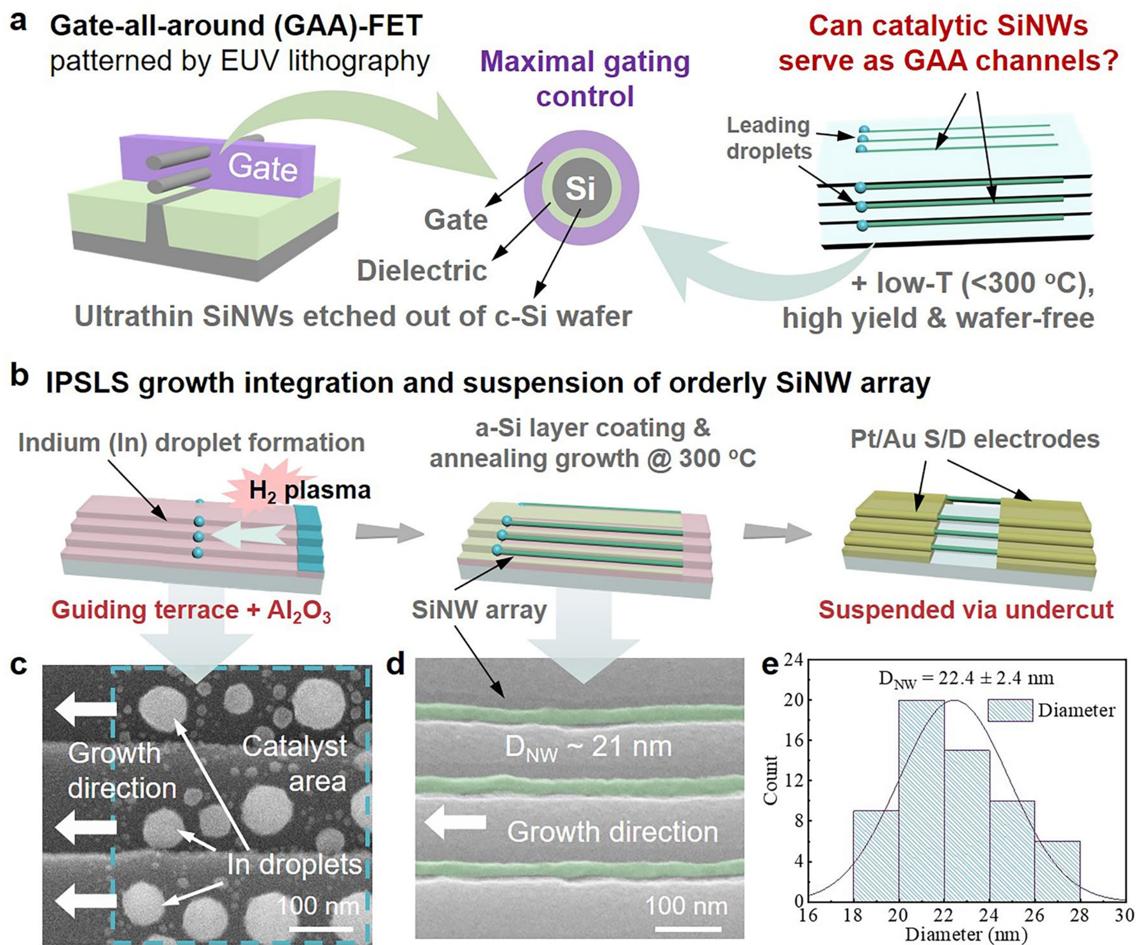


Fig. 1 **a** Schematic illustration of GAA structure fabricated via EUV lithography and etching and catalytic growth integration, **b** IPSLS growth integration and suspension of orderly SiNW array, typical SEM images of **c** the catalyst area and **d** as-grown SiNWs, **e** statistics on the diameter of as-grown ultrathin IPSLS SiNWs

droplets with diameters of 70 ± 11 nm, as witnessed in the scanning electron microscopy (SEM) image in Fig. 1c; (2) the deposition of 7 nm thick a-Si precursor film over the whole sample surface at a lower temperature at 110 °C (below the In melting point), followed by annealing in vacuum after raising the substrate temperature to 290 °C, which activated the droplets to absorb the a-Si layer, move along the terrace steps, and produce ultrathin SiNWs. At the end, the source/drain (S/D) electrode pads, of a bilayer of platinum (Pt)/gold (Au) of 12/55 nm thick, were patterned by using electron beam lithography (EBL) and deposited by electron beam evaporation.

In order to release the SiNWs to form suspended channels, the exposed sacrificial Al_2O_3 layer, uncovered by the S/D pads, was etched off by immersing in diluted alkaline solutions (2.5%), and more experimental details are provided in the Supporting Information. According to a typical SEM image of the as-grown SiNWs presented in Fig. 1d, the parallel SiNWs, pseudo-colored in green for the sake of clarity, show a uniform diameter of approximately 21 nm and are well positioned at the roots of the mini-steps of the guiding terrace. Note that, a high uniformity of the as-grown SiNWs, with an average diameter of D_{NW}= 22.4 ± 2.4 nm, has been achieved here mainly through the In thickness control and subsequent droplets formation [22], as witnessed in the statistics shown in Fig. 1e.

Figure 2a summarizes the whole fabrication procedure, where the key steps of forming suspended SiNW channels that is the undercut-releasing and dielectric deposition steps,

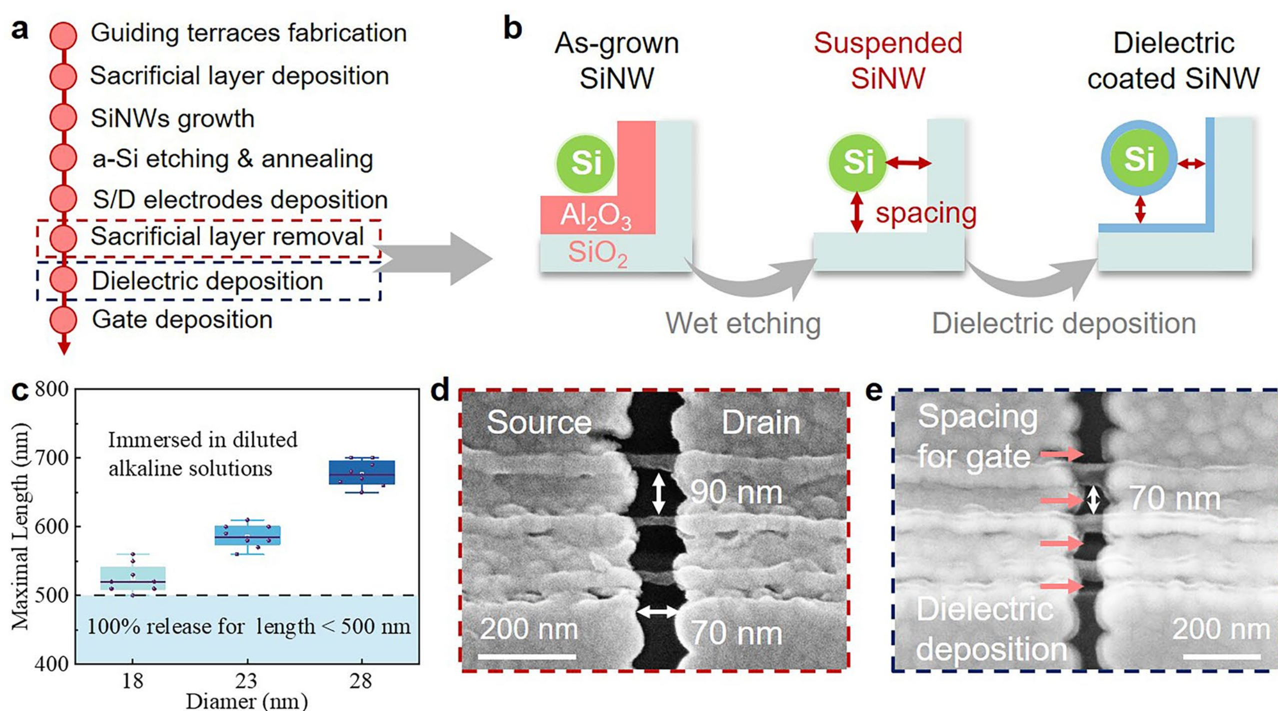


Fig. 2 **a** Fabrication processes of SiNW GAA-FETs, **b** schematic illustrations of the undercut-releasing and dielectric deposition steps. **c** Statistics on the maximum suspension length for the SiNW channels of different diameters. **d–e** Typical SEM images of the suspended SiNWs, held by S/D electrode pads, before and after dielectric deposition of 3 nm Al_2O_3 and 7 nm HfO_2

have been highlighted by two dash rectangles. Specifically, a rather conformal Al_2O_3 sacrificial layer of 40 nm thick has been coated on the terrace surface, by using ALD, which can be safely removed by immersing in a diluted alkaline solution, as depicted in Fig. 2b, leaving a suspended array of SiNW channels held by the S/D metal pads at the two ends. Despite such a simple solution etching-releasing procedure, without using a supercritical releasing technique [34], this Al_2O_3-alkaline undercutting has proven to be gentle enough to presume the geometry and integrity of the suspended SiNWs. For example, Fig. S1 presents the SEM images of the well-released and suspended SiNWs with spanning lengths of 100, 250, 310, 460, and even up to 700 nm, respectively. For even longer suspension lengths, the SiNWs were found to either attach to the substrate or break, being dragged down by the retracting liquid interfacial force as they were pulled out of the etching solution.

The maximum suspension length is also correlated with the diameter of SiNW, as evidenced in the statistics presented in Fig. 2c. For example, SiNWs with the largest diameter of 28 nm can be successfully released to form suspended channels throughout 700 nm with a 100% survival rate. In contrast, the thinnest SiNWs, with diameters of 18 nm, can only be safely released over a suspension length of less than 500 nm. However, even this shorter length is sufficient for suspending the SiNWs to serve as GAA-FET channels. After undercut-releasing three parallel SiNWs as channels, to form a suspended channel length of $L_{nw} \sim 70$ nm, with a close interwire spacing of 90 nm, as seen in Fig. 2d, a uniform stacked dielectric layer of 3 nm Al_2O_3 and 7 nm HfO_2 was deposited by using ALD (Fig. 2e). It is important to note that the SiNWs are now suspended at a distance of 40 nm from both the substrate and the sidewall, determined by the thickness of the sacrificial Al_2O_3 layer. This separation provides sufficient space for applying the dielectric deposition and the subsequent wrapping of the gate metal, which is a critical requirement for fabricating a genuine gate-all-around (GAA) FET device.

After the dielectric layer deposition step, the suspended SiNW channels were covered with the gating electrode, resulting in a typical GAA configuration. In comparison, a reference FET with grounded SiNW channels, unreleased ones resided at the roots of step corners, was also prepared. Figure 3a, b shows the cross-sectional high-resolution

© The authors https://doi.org/10.1007/s40820-025-01674-8

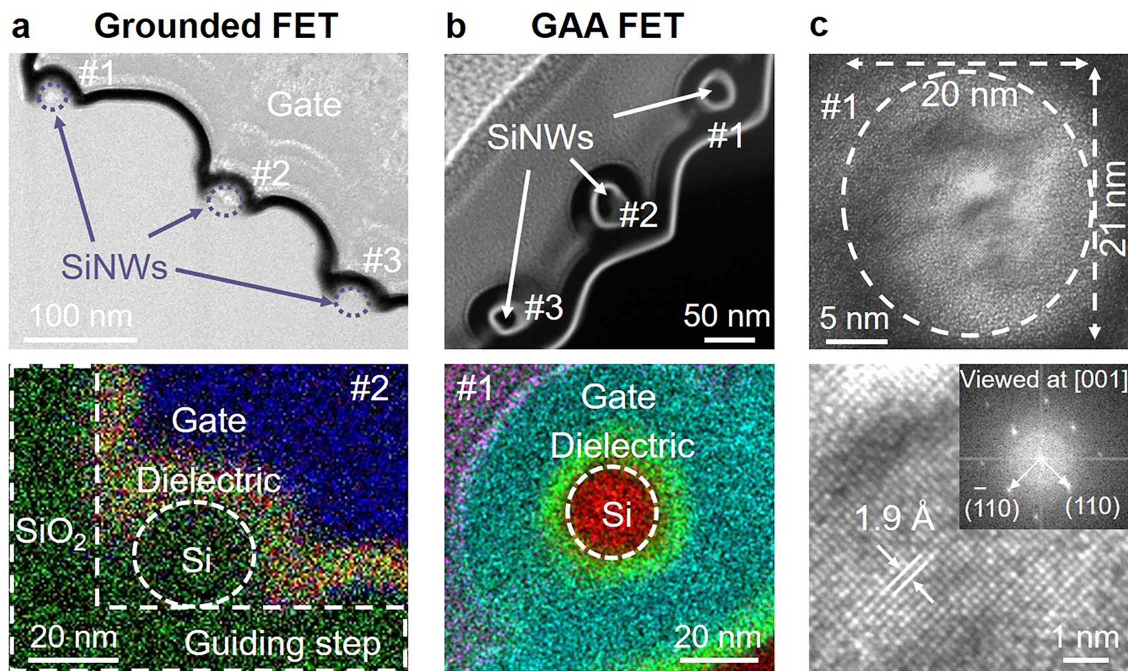


Fig. 3 Cross-section TEM images and corresponding high-resolution EDS maps of the IPSLS SiNW-FETs: **a** Grounded and **b** GAA-FET. **c** Enlarged HR-TEM images and corresponding electron diffraction pattern of #1 SiNWs in GAA-FET

transmission electron microscopy (HR-TEM) analysis of the grounded and released (GAA) SiNW channels, respectively. It is important to note that, according to the detailed SEM inspections and EDS (energy-dispersive spectroscopy) mapping of the exposed channel cross sections, the grounded SiNW channels (seen in Fig. 3a) can only be effectively gated by the gate electrode from the top and the right sides, limited geometrically by the concave step corner sidewalls. In contrast, in a GAA configuration, as shown in Fig. 3b, the SiNW channels can be fully wrapped around and gated in all directions to achieve the maximum capacitive gate-channel coupling. Furthermore, as illustrated in Fig. 3c, the enlarged HR-TEM image reveals a slightly ellipsoidal SiNW, with a height and width of approximately 20 and 21 nm, respectively. This particular SiNW has been found to be monocrystalline with a clear lattice fringe spacing of 0.19 nm, corresponding to that of the Si (110) planes. Meanwhile, the fast Fourier transform (FFT) pattern displayed in the inset indicates that the growth direction of this specific SiNW is along Si < 100 >, while Si < 110 > is more commonly observed according to the statistics of growth orientations in Fig. S2, as well as those shown in our previous works [23, 24].

Figure 4a presents an SEM image of the as-fabricated GAA-FET, with a channel length of 300 nm and a pair of source/drain (S/D) contact electrodes of Pt (12 nm)/Au (55 nm). As illustrated in Fig. 4b, under a bias of $V_{DS} = -0.1$ V, the GAA-FET demonstrates a high I_{ON}/I_{OFF} ratio of 10^7, a sharp SS of 66 mV dec^{-1} and a low leakage current < 0.1 pA (corresponding to an off-state power consumption < 0.03 pW and a conductive power consumption of ~ 0.2 μW). In comparison, the reference FET with grounded SiNW channels exhibits an I_{ON}/I_{OFF} ratio of $< 10^6$ and a higher SS = 150 mV dec^{-1}. More systematic comparison of the SS performance evolution trends of the GAA- or grounded FETs, at different channel current loads and biases (as depicted in Figs. 4d and S3), are staged in Fig. 4c, e, respectively. It is found that the GAA configuration can indeed largely enhance the field-effect gating efficiency of the SiNW-FET, achieving a much lower SS approaching the theoretical limit of 60 mV dec^{-1} [35]. In addition, the transfer characteristics of 20 randomly selected SiNW GAA-FETs are depicted in Fig. S4, where all devices show an average $I_{on/off}$ current ratio > 10^6 under a bias of $V_{DS} = -0.1$ V. The SS values, ranging from 64 to 85 mV dec^{-1}, are also comparable to those observed in the cutting-edge top-down GAA-FET devices [26, 36–38].

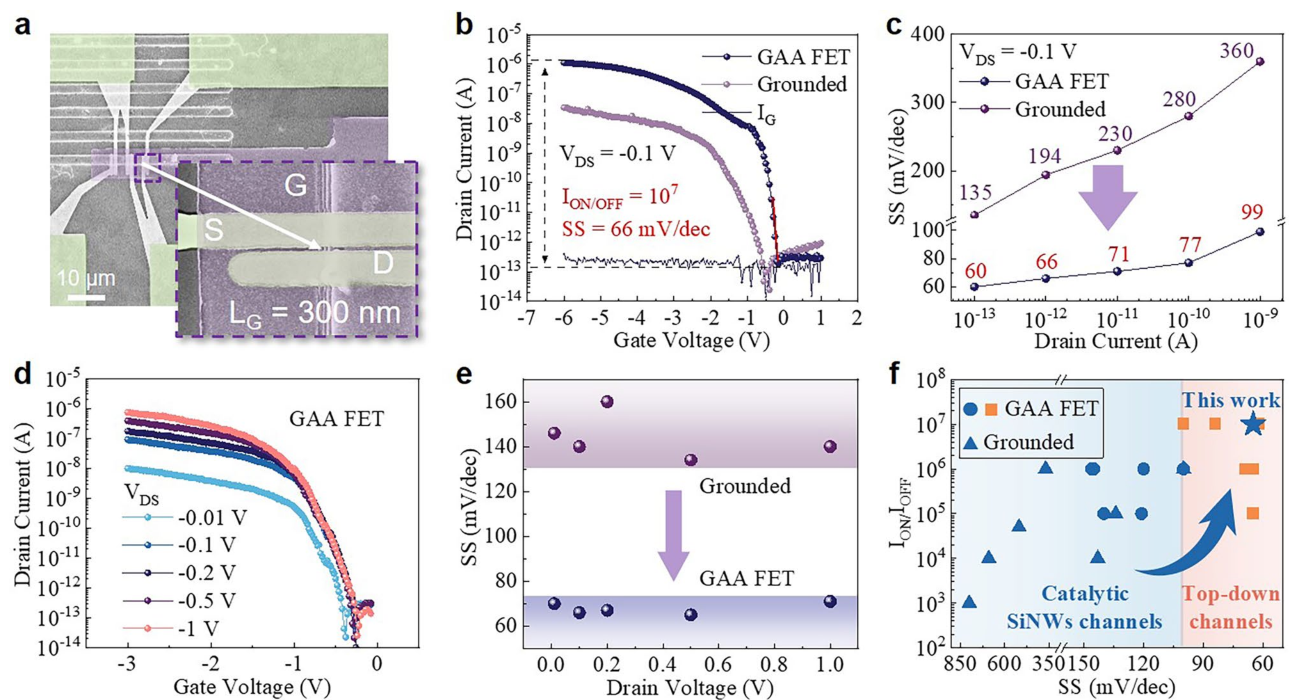


Fig. 4 **a** SEM images of the GAA-FET. **b** $I_D - V_G$ curves ($V_D = 0.1$ V) and **c** $SS - I_D$ curves of grounded FET and GAA-FET. **d** Typical transfer curves of GAA-FET. **e** $SS - V_D$ curves of grounded FET and GAA-FET. **f** Comparison of the SS and I_{ON}/I_{OFF} ratio of FETs based on catalytic SiNW [10, 11, 16, 17, 27–33, 40] and top-down etched SiNW/NS [26, 36–38, 41, 42] in the literature

This finding also emphasizes the fact that a more efficient gating configuration is required to fulfill the potential of the catalytic SiNWs to serve as the 1D channels for high-performance FETs. One of the major reasons for the insufficient gating control of the SiNW can be assigned to the relatively high indium (In) atom density incorporated into the SiNWs during the IPSLS growth, which is known to introduce *p*-type doping in c-Si and has been verified to be $n_{In} \sim 10^{19}$ cm^{-3} in the as-grown SiNWs in our previous works [33, 39]. Though the dissolved In atom density can be substantially reduced via a post-growth annealing to below 10^{16} cm^{-3}, a more straight strategy is to reduce the diameter of the SiNW channel, to be smaller than the Debye screening length of the In-doped SiNWs, $D_{nw} < \lambda$, where $\lambda \sim n_{In}^{-1/2}$ is in the order of ~ 10 nm for a doping concentration of 10^{16} cm^{-3}. However, in the GAA-FET configuration, the field-effect gating can be applied from all directions, and thus this Debye screening length restriction can be extended to $D_{nw}/2 < \lambda$. Or, in other words, the carrier density in SiNW can be more effectively modulated to achieve a far more efficient channel current switching control, to achieve a lower SS ~ 60 mV dec^{-1}, approaching the theoretical limit.

On the other hand, it is also important to note that, there is no doping in the S/D contact regions and SiNW-FETs demonstrated here are in a convenient junctionless configuration. So, the choice of suitable S/D contact metals, with the right work function that matches the doping style and concentration in the SiNW channels, is another key control parameter to obtain a lower contact resistance to boost the drive current. Here, GAA-FETs with Ti/Au (12/55 nm) or Pt/Au (12/55 nm) as S/D contact electrodes were fabricated and compared. As shown in the typical transfer curves shown in Fig. 5a–d, the Ti/Au contacted GAA device delivers a lower on–off current ratio of only 10^3, despite a sharp SS of 62 mV dec^{-1} has been recorded at the early turning-on regime. In comparison, with basically identical GAA channel conditions, the Pt/Au contacted GAA-FET exhibits a remarkable increase in on current by nearly four orders of magnitude, achieving simultaneously high $I_{on/off} = 10^7$ and an SS = 65 mV dec^{-1}. Note that, both of the GAA-FETs demonstrate a negligible hysteresis in forward and backward sweeps, but with slightly higher SS in backward track.

© The authors https://doi.org/10.1007/s40820-025-01674-8

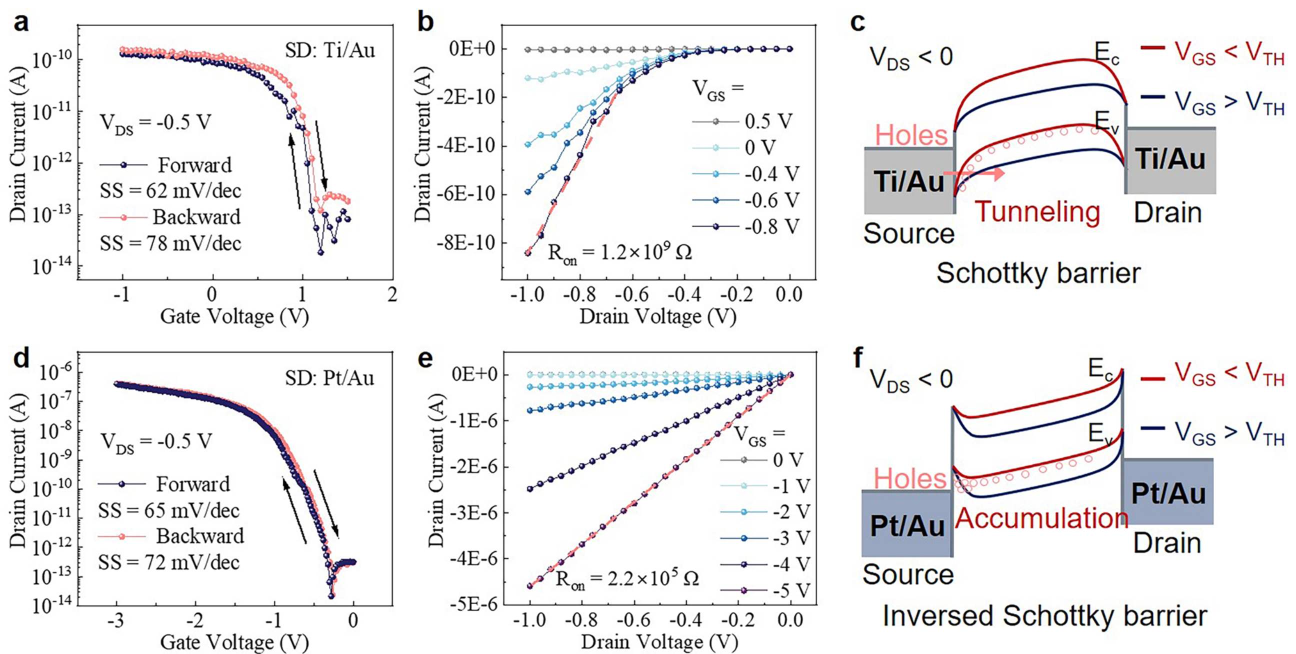


Fig. 5 **a** Hysteresis curves and **b** output curves of the Ti/Au contacted GAA-FET, **c** corresponding band gap alignment profiles under different gating bias conditions, where a large Schottky barrier is formed at the Ti/SiNW contact, **d** hysteresis curves and **e** output curves of the Pt/Au contacted GAA-FET, **f** corresponding band gap alignment profiles under different gating bias conditions, where the Pt/SiNW contact forms an inverse Schottky barrier

According to the output characteristics presented in Fig. 5b–e, it is evident that the Pt/Au contacted SiNW-FETs behave more like Ohmic contact than the Ti/Au contacted ones. Specifically, the on-state resistance (R_{on}) of the Pt/Au contacted SiNW-FET (2.2×10^5 Ω) is reduced by more than three orders of magnitude relative to that of the Ti/Au contacted device (1.2×10^9 Ω). This phenomenon can be attributed to the different work functions of the primary contact metals of Ti and Pt. As illustrated in the energy band diagrams of Fig. 5c, f, a work function of Ti is about 4.3 eV, 0.2 eV higher than the valence band top of c-Si, and thus will tend to pull up the band profile of c-SiNW channel to create a large Schottky barrier at the Ti/SiNW contact. To turn on the SiNW channel connected by a pair of back-to-back Schottky barriers, a negative gating voltage of $V_{GS} < V_{TH}$ is required to force the triangle Schottky barrier to become thinner and thinner, to allow for direct hole tunneling. However, the existence of such Schottky barriers poses a fundamental limit for the transport current, particularly in high current on state, as evidenced in Fig. 5a. So, by choosing a metal with deeper work function of approximately 5.6 eV for Pt, this situation can be greatly facilitated. As diagrammed in Fig. 5f, the Pt/p-SiNW contact forms an inverse Schottky barrier, and thus makes it possible to boost the on current of the GAA-FETs.

As summarized in Fig. 4f, although catalytic SiNWs have been widely investigated as promising channel materials for high-performance FETs over the last two decades, their subthreshold swing (SS) performances have typically been limited to a range of 850–100 mV dec^{-1} [27–33]. Among them, SiNW-FETs with GAA gating have achieved, on average, a higher on/off ratio up to 10^6 and a smaller SS approaching 100 mV dec^{-1} [10, 11, 16, 17, 40], as represented by the filled blue circles. This limit has now been broken in this work, with the ultrathin SiNW GAA-FETs denoted by a blue star, which stand in the upper-right corner of the high-performance region in Fig. 4f (with $I_{on/off} > 10^7$ and SS < 90 mV dec^{-1}). This region has long been occupied only by the cutting-edge fin or GAA gate FETs marked by the orange rectangles [26, 36–38, 41, 42].

This comparison can be better understood with more technical details, as provided in Table 1. The catalytic SiNWs, grown primarily through the most popular VLS mechanism,

typically exhibit a larger diameter and less stringent uniformity control, usually ranging from 30 to 150 nm. The relatively thicker diameter and larger diameter variation of the VLS-grown SiNWs are major reasons for the poorer channel current modulation efficiency, and thus higher SS of the VLS-SiNW-FETs, even fabricated in a GAA gating configuration. More importantly, vertically grown VLS SiNWs are difficult to integrate into the mainstream planar device architecture, and thus necessitating a complex post-transfer and re-arrangement of the tiny individual SiNWs for the subsequent fabrication of GAA-FETs. On the other hand, in contrast to the standard top-down fin or GAA gate FETs, most of the SiNW-FETs, including those in this work, are fabricated with a junctionless S/D metal contact. This thus requires a careful choice of suitable S/D contact metals to match the channel doping polarity in the SiNW channels. Otherwise, the formation of a pair of Schottky barriers at the S/D contact will seriously degrade the electronic transport performance, as already evidenced here.

With that said, the role of catalytic SiNWs in the development of high-performance GAA-FETs should not be discounted. On the contrary, our results provide straightforward experimental evidence that, with ultrathin and uniform diameter control and appropriate S/D contact, GAA-FETs built upon catalytic SiNW can also achieve excellent FET performance comparable to those fabricated with cutting-edge top-down lithography technology. Compared to the traditional GAA-FET fabrication that relies on sophisticated EUV/EBL lithography to pattern/define ultrathin c-Si channels (< 20 nm) out of Si/SiGe superlattice multilayers deposited on c-Si wafer, these catalytic SiNWs can be grown as orderly arrays at low temperatures (< 300 °C) upon dielectric substrate, without the need of the pre-existing c-Si wafer and the use of high-precision lithography [24]. All these unique features of IPSLS catalytic SiNWs make them particularly suited for constructing a new generation of 3D integrated electronics or computing-in-memory applications. Compared to the commonly used channel materials for monolithic 3D integrations, such as amorphous oxide semiconductor (AOS), low-dimensional materials, and poly-Si-based FETs reported in the literature and summarized in Table S1, the SiNW GAA-FET also demonstrates a superior performance in terms of SS and on–off current ratio [43–53].

However, it is equally important to point out that the catalytic SiNW channels still need to improve in terms of size and lattice uniformity, compared to the stringent parameter control achieved in standard top-down etched GAA channels. Also, the SiNW array fabricated here is not arranged in a high-density stacked manner as in the standard GAA-FET configuration [26, 38, 42]. So, a sidewall groove-guided growth integration of even thinner SiNWs, as demonstrated in our previous works [23, 24], still needs to be testified to improve further the channel integration density. Moreover, the contact resistance under the metal-SiNW S/D electrode also needs to be reduced by suitable doping control or ion-implantation technique. To this end, the a-Si precursor pre-doping control strategy, established in our previous works [54], can help to adjust the effective

Table 1 Comparison of our GAA-FET to the SiNW/NS GAA-FETs in other literature

Fabrication strategies		D_{NW} or CD* (nm)	I_{ON} (A)	I_{ON}/I_{OFF}	$\|V_D\|$ (V)	SS (mV dec^{-1})	References
Top-down etching	EBL	7–18	10^2	10^5	1	140	[41]
	EBL	8	10^{-6}	10^7	0.1	62	[36]
	EBL	8–10	10^{-5}	10^7	1	84	[37]
	Edge mask	6	10^{-6}	10^5	0.9	65.1	[38]
	Edge mask	8	10^{-4}	10^6	0.7	69.2	[42]
	EUV lithography	4	10^{-6}	10^6	0.65	65	[26]
Catalytic growth	VLS (V-FET)	20–30	10^{-7}	10^6	0.25	120	[10]
	VLS and transfer	25–60	10^{-7}	10^6	0.5	105	[11]
	VLS and transfer	20–120	10^{-8}	10^5	1	121	[16]
	VLS and transfer	100–150	10^{-6}	10^6	0.95	145	[17]
	VLS over trench	120–150	10^{-7}	10^6	0.05	146	[40]
	IPSLS	22.4 ± 2.4	10^{-6}	10^7	0.1	66	This work

*Critical dimension: the smallest thickness/width of nanosheet channels

© The authors https://doi.org/10.1007/s40820-025-01674-8

channel doping and ameliorate the S/D contact. Finally, a complementary n-type GAA-FET has yet to be demonstrated in our future work for building high-density CMOS logic with reduced contacted gate pitch.

3 Conclusion

In summary, we have demonstrated high-performance GAA-FETs based on catalytic IPSLS SiNWs, which can be grown into orderly arrays, with ultrathin diameters of $D_{NW} = 22.4 \pm 2.4$ nm and close interwire spacing of 90 nm. A series of undercut-releasing and optimized S/D contact techniques have been successfully developed to establish reliable and scalable fabrication protocols of GAA-FET logic. For the first time, the electronic transport performance of junctionless FETs with catalytic SiNW channels has been largely improved, achieving an excellent $I_{on/off}$ current ratio of 10^7 and a steep SS of 66 mV dec^{-1}, comparable to those fabricated with the aid of top-down EBL and EUV lithography. These results represent the first experimental evidence that the catalytic SiNWs grown via a low-temperature IPSLS process hold important potential for building state-of-the-art high-performance GAA-FETs, particularly suited for monolithic 3D integrations.

Acknowledgements The authors acknowledge the financial support received from the National Key Research Program of China under granted No. 92164201, the National Natural Science Foundation of China for Distinguished Young Scholars No. 62325403, the Fundamental Research Funds for the Central Universities, and the National Natural Science Foundation of China under No.61934004.

Authors' Contribution Wei Liao contributed to investigation, methodology, formal analysis, data curation, original draft writing. Wentao Qian, Lei Liang, Zhiyan Hu and Junyang An contributed to methodology. Junzhuan Wang contributed to funding acquisition, conceptualization. Linwei Yu contributed to investigation, resources, original draft writing, review, funding acquisition, conceptualization.

Declarations

Conflict of Interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Open Access This article is licensed under a Creative Commons Attribution 4.0 International License, which permits use, sharing, adaptation, distribution and reproduction in any medium or format, as long as you give appropriate credit to the original author(s) and the source, provide a link to the Creative Commons licence, and indicate if changes were made. The images or other third party material in this article are included in the article's Creative Commons licence, unless indicated otherwise in a credit line to the material. If material is not included in the article's Creative Commons licence and your intended use is not permitted by statutory regulation or exceeds the permitted use, you will need to obtain permission directly from the copyright holder. To view a copy of this licence, visit http://creativecommons.org/licenses/by/4.0/.

Supplementary Information The online version contains supplementary material available at https://doi.org/10.1007/s40820-025-01674-8.

References

1. S. Bangsaruntip, G.M. Cohen, A. Majumdar, Y. Zhang, S.U. Engelmann et al., *High Performance and Highly Uniform Gate-All-Around Silicon Nanowire MOSFETs with Wire Size Dependent Scaling*. 2009 IEEE international electron devices meeting (IEDM). December 7–9, 2009, Baltimore, (IEEE, 2009), pp. 1–4
2. G. Bae, D.I. Bae, M. Kang, S.M. Hwang, S.S. Kim et al., *3nm GAA Technology Featuring Multi-bridge-channel FET for Low Power and High Performance Applications*. 2018 IEEE international electron devices meeting (IEDM). 28.27.21–28.27.24 (2018). https://doi.org/10.1109/IEDM.2018.8614629
3. S. Liao, L. Yang, T.K. Chiu, W.X. You, T.Y. Wu et al., *Complementary Field-Effect Transistor (CFET) Demonstration at 48nm Gate Pitch for Future Logic Technology Scaling*. 2023 International electron devices meeting (IEDM). pp. 1–4, (2023). https://doi.org/10.1109/iedm45741.2023.10413672
4. L. Qin, C. Li, Y. Wei, G. Hu, J. Chen et al., Recent developments in negative capacitance gate-all-around field effect transistors: a review. IEEE Access **11**, 14028–14042 (2023). https://doi.org/10.1109/ACCESS.2023.3243697
5. C.-C. Yang, T.-Y. Hsieh, W.-H. Huang, C.-H. Shen, J.-M. Shieh et al., Recent progress in low-temperature-process monolithic three dimension technology. Jpn. J. Appl. Phys. **57**, 04FA06 (2018). https://doi.org/10.7567/jjap.57.04fa06
6. P. Lin, C. Li, Z. Wang, Y. Li, H. Jiang et al., Three-dimensional memristor circuits as complex neural networks. Nat. Electron. **3**, 225–232 (2020). https://doi.org/10.1038/s41928-020-0397-9
7. Q. Zhang, Y. Zhang, Y. Luo, H. Yin, New structure transistors for advanced technology node CMOS ICs. Natl. Sci. Rev. **11**, nwae008 (2024). https://doi.org/10.1093/nsr/nwae008
8. L. Liang, R. Hu, L. Yu, Toward monolithic growth integration of nanowire electronics in 3D architecture: a review. Sci. China Inf. Sci. **66**, 200406 (2023). https://doi.org/10.1007/s11432-023-3774-y
9. Q. Hua, G. Shen, Low-dimensional nanostructures for monolithic 3D-integrated flexible and stretchable electronics.

Chem. Soc. Rev. **53**, 1316–1353 (2024). https://doi.org/10.1039/d3cs00918a
10. J. Goldberger, A.I. Hochbaum, R. Fan, P. Yang, Silicon vertically integrated nanowire field effect transistors. Nano Lett. **6**, 973–977 (2006). https://doi.org/10.1021/nl060166j
11. O. Shirak, O. Shtempluck, V. Kotchtakov, G. Bahir, Y.E. Yaish, High performance horizontal gate-all-around silicon nanowire field-effect transistors. Nanotechnology **23**, 395202 (2012). https://doi.org/10.1088/0957-4484/23/39/395202
12. P. Namdari, H. Daraee, A. Eatemadi, Recent advances in silicon nanowire biosensors: synthesis methods, properties, and applications. Nanoscale Res. Lett. **11**, 406 (2016). https://doi.org/10.1186/s11671-016-1618-z
13. H. Li, D. Li, H. Chen, X. Yue, K. Fan et al., Application of silicon nanowire field effect transistor (SiNW-FET) biosensor with high sensitivity. Sensors **23**, 6808 (2023). https://doi.org/10.3390/s23156808
14. C. Jia, Z. Lin, Y. Huang, X. Duan, Nanowire electronics: from nanoscale to macroscale. Chem. Rev. **119**, 9074–9135 (2019). https://doi.org/10.1021/acs.chemrev.9b00164
15. T. Arjmand, M. Legallais, T.T.T. Nguyen, P. Serre, M. Vallejo-Perez et al., Functional devices from bottom-up silicon nanowires: a review. Nanomaterials **12**, 1043 (2022). https://doi.org/10.3390/nano12071043
16. J.-H. Lee, B.-S. Kim, S.-H. Choi, Y. Jang, S.W. Hwang et al., A facile route to Si nanowire gate-all-around field effect transistors with a steep subthreshold slope. Nanoscale **5**, 8968–8972 (2013). https://doi.org/10.1039/C3NR02552G
17. B. Salem, G. Rosaz, N. Pauc, P. Gentile, P. Periwal et al., *Electrical Characterisation of Horizontal and Vertical Gate-All-Around Si/SiGe Nanowires Field Effect Transistors*. 2014 Silicon nanoelectronics workshop (SNW). June 8–9, 2014, Honolulu, (IEEE, 2014), pp. 1–2
18. L. Yu, P.-J. Alet, G. Picardi, Pere Roca i Cabarrocas, An in-plane solid-liquid-solid growth mode for self-avoiding lateral silicon nanowires. Phys. Rev. Lett. **102**, 125501 (2009). https://doi.org/10.1103/PhysRevLett.102.125501
19. M. Xu, Z. Xue, L. Yu, S. Qian, Z. Fan et al., Operating principles of in-plane silicon nanowires at simple step-edges. Nanoscale **7**, 5197–5202 (2015). https://doi.org/10.1039/c4nr06531j
20. Z. Xue, M. Sun, T. Dong, Z. Tang, Y. Zhao et al., Deterministic line-shape programming of silicon nanowires for extremely stretchable springs and electronics. Nano Lett. **17**, 7638–7646 (2017). https://doi.org/10.1021/acs.nanolett.7b03658
21. S. Xu, R. Hu, J. Wang, Z. Li, J. Xu et al., Terrace-confined guided growth of high-density ultrathin silicon nanowire array for large area electronics. Nanotechnology **32**, 265602 (2021). https://doi.org/10.1088/1361-6528/abf0c9
22. W. Liao, Y. Zhang, D. Li, J. Wang, L. Yu, High-density integration of uniform sub-22 nm silicon nanowires for transparent thin film transistors on glass. Appl. Surf. Sci. **679**, 161213 (2025). https://doi.org/10.1016/j.apsusc.2024.161213
23. R. Hu, S. Xu, J. Wang, Y. Shi, J. Xu et al., Unprecedented uniform 3D growth integration of 10-layer stacked Si nanowires on tightly confined sidewall grooves. Nano Lett. **20**, 7489–7497 (2020). https://doi.org/10.1021/acs.nanolett.0c02950
24. R. Hu, Y. Liang, W. Qian, X. Gan, L. Liang et al., Ultra-confined catalytic growth integration of sub-10 nm 3D stacked silicon nanowires *via* a self-delimited droplet formation strategy. Small **18**, e2204390 (2022). https://doi.org/10.1002/smll.202204390
25. Y. Cheng, Z. Liu, J. Wang, J. Xu, L. Yu, Deterministic single-row-droplet catalyst formation for uniform growth integration of high-density silicon nanowires. ACS Appl. Mater. Interfaces **16**, 23625 (2024). https://doi.org/10.1021/acsami.4c03991
26. M. Radosavljevic, C.Y. Huang, W. Rachmady, S.H. Seung, N.K. Thomas et al., *Opportunities in 3-D Stacked cmos Transistors*. 2021 IEEE international electron devices meeting (IEDM). 34.31.31–34.31.34 (2021). https://doi.org/10.1109/iedm19574.2021.9720633
27. V. Brouzet, B. Salem, P. Periwal, G. Rosaz, T. Baron et al., Fabrication and characterization of silicon nanowire p-i-n MOS gated diode for use as p-type tunnel FET. Appl. Phys. A **121**, 1285–1290 (2015). https://doi.org/10.1007/s00339-015-9507-3
28. S. Glassner, C. Zeiner, P. Periwal, T. Baron, E. Bertagnolli et al., Multimode silicon nanowire transistors. Nano Lett. **14**, 6699–6703 (2014). https://doi.org/10.1021/nl503476t
29. A.L. Vallett, S. Minassian, P. Kaszuba, S. Datta, J.M. Redwing et al., Fabrication and characterization of axially doped silicon nanowire tunnel field-effect transistors. Nano Lett. **10**, 4813–4818 (2010). https://doi.org/10.1021/nl102239q
30. K.E. Moselund, H. Ghoneim, M.T. Björk, H. Schmid, S. Karg et al., *VLS-grown Silicon Nanowire Tunnel FET.*2009 device research conference. June 22-24, 2009, University Park, (IEEE, 2009), pp. 23–24
31. M.T. Björk, J. Knoch, H. Schmid, H. Riel, W. Riess, Silicon nanowire tunneling field-effect transistors. Appl. Phys. Lett. **92**, 193504 (2008). https://doi.org/10.1063/1.2928227
32. M. Xu, Z. Xue, J. Wang, Y. Zhao, Y. Duan et al., Heteroepitaxial writing of silicon-on-sapphire nanowires. Nano Lett. **16**, 7317–7324 (2016). https://doi.org/10.1021/acs.nanolett.6b02004
33. L. Yu, W. Chen, B. O'Donnell, G. Patriarche, S. Bouchoule et al., Growth-in-place deployment of in-plane silicon nanowires. Appl. Phys. Lett. **99**, 203104 (2011). https://doi.org/10.1063/1.3659895
34. Z. Liu, J. Yan, H. Ma, T. Hu, J. Wang et al., *Ab initio* design, shaping, and assembly of free-standing silicon nanoprobes. Nano Lett. **21**, 2773–2779 (2021). https://doi.org/10.1021/acs.nanolett.0c04804
35. K.W. Frese, C. Chen, Theoretical models of hot carrier effects at metal-semiconductor electrodes. J. Electrochem. Soc. **139**, 3234–3243 (1992). https://doi.org/10.1149/1.2069059
36. S.W. Chang, P.J. Sung, T.Y. Chu, D.D. Lu, C.J. Wang et al., *First Demonstration of cmos Inverter and 6T-SRAM Based*

on GAA CFETs Structure for 3D-IC Applications. 2019 IEEE International electron devices meeting (IEDM), 11.17.11–11.17.14 (2019). https://doi.org/10.1109/IEDM19573.2019.8993525

37. F.-K. Hsueh, J.-M. Hung, S.-P. Huang, Y.-H. Huang, C.-X. Xue et al., *First Demonstration of Ultrafast Laser Annealed Monolithic 3D Gate-All-Around CMOS Logic and FeFET Memory with Near-Memory-Computing macro*. 2020 IEEE International electron devices meeting (IEDM). December 12–18, 2020, San Francisco, (IEEE, 2020), 40.4.1–40.4.4
38. J. Yao, Y. Wei, S. Yang, H. Yang, G. Xu et al., *Record 7(N) 7(P) Multiple VTs Demonstration on gaa si Nanosheet n/pFETs Using WFM-Less Direct Interfacial La/Al-Dipole Technique*. 2022 International electron devices meeting (IEDM). December 3–7, 2022, San Francisco, (IEEE, 2022), 34.2.1–34.2.4
39. W. Chen, L. Yu, S. Misra, Z. Fan, P. Pareige et al., Incorporation and redistribution of impurities into silicon nanowires during metal-particle-assisted growth. Nat. Commun. **5**, 4134 (2014). https://doi.org/10.1038/ncomms5134
40. J.Y. Oh, J.T. Park, H.J. Jang, W.J. Cho, M.S. Islam, 3D-transistor array based on horizontally suspended silicon nano-bridges grown *via* a bottom-up technique. Adv. Mater. **26**, 1929–1934 (2014). https://doi.org/10.1002/adma.201304245
41. Y. Song, H. Zhou, Q. Xu, J. Niu, J. Yan et al., High-performance silicon nanowire gate-all-around nMOSFETs fabricated on bulk substrate using CMOS-compatible process. IEEE Electron Device Lett. **31**, 1377–1379 (2010). https://doi.org/10.1109/LED.2010.2080256
42. X. Zhang, J. Yao, Y. Luo, L. Cao, Y. Zheng et al., Hybrid integration of gate-all-around stacked Si nanosheet FET and Si/*SiGe* super-lattice FinFET to optimize 6T-SRAM for N3 node and beyond. IEEE Trans. Electron Devices **71**, 1776–1783 (2024). https://doi.org/10.1109/TED.2024.3358251
43. Y. Son, B. Frost, Y. Zhao, R.L. Peterson, Monolithic integration of high-voltage thin-film electronics on low-voltage integrated circuits using a solution process. Nat. Electron. **2**, 540–548 (2019). https://doi.org/10.1038/s41928-019-0316-0
44. Q. Li, J. Dong, D. Han, J. Wang, D. Xu et al., Back-end-of-line compatible InSnO/ZnO heterojunction thin-film transistors with high mobility and excellent stability. IEEE Electron Device Lett. **43**, 1251–1254 (2022). https://doi.org/10.1109/LED.2022.3185099
45. S. Hooda, M. Lal, C. Chun-Kuei, S.-H. Tsai, E. Zamburg et al., BEOL compatible extremely scaled bilayer ITO/IGZO channel FET with high mobility 106 cm^2/V.s. 2023 7th IEEE electron devices technology & manufacturing conference (EDTM). March 7-10, 2023, Seoul, (IEEE, 2023), pp. 1–4
46. Q. Smets, G. Arutchelvan, J. Jussot, D. Verreck, I. Asselberghs et al., Ultra-scaled MOCVD MoS_2 MOSFETs with 42nm contact pitch and 250µA/µm drain current. 2019 IEEE International electron devices meeting (IEDM). December 7–11, 2019, San Francisco, (IEEE, 2019), 23.2.1–23.2.4
47. X. Huang, C. Liu, Z. Tang, S. Zeng, L. Liu et al., *High Drive and Low Leakage Current MBC FET with Channel Thickness 1.2 nm/0.6 nm*. 2020 IEEE International electron devices meeting (IEDM). December 12–18, 2020, San Francisco, (IEEE, 2020), 12.1.1–12.1.4
48. Y.Y. Chung, B.J. Chou, C.F. Hsu, W.S. Yun, M.Y. Li et al., *First Demonstration of GAA Monolayer-MoS_2 Nanosheet nFET with 410 µA/µm I_D at 1V V_D at 40 nm Gate Length*. 2022 International electron devices meeting (IEDM). 34.35.31–34.35.34 (2022). https://doi.org/10.1109/IEDM45625.2022.10019563
49. F. Wu, H. Tian, Y. Shen, Z. Hou, J. Ren et al., Vertical MoS_2 transistors with sub-1-nm gate lengths. Nature **603**, 259–264 (2022). https://doi.org/10.1038/s41586-021-04323-3
50. R. Pendurthi, N.U. Sakib, M.U.K. Sadaf, Z. Zhang, Y. Sun et al., Monolithic three-dimensional integration of complementary two-dimensional field-effect transistors. Nat. Nanotechnol. **19**, 970–977 (2024). https://doi.org/10.1038/s41565-024-01705-2
51. C.-C. Yang, T.-Y. Hsieh, P.-T. Huang, K.-N. Chen, W.-C. Wu et al., *Location-Controlled-Grain Technique for Monolithic 3D BEOL FinFET Circuits*. 2018 IEEE International Electron Devices Meeting (IEDM). December 1–5, 2018, San Francisco. (IEEE 2018), 11.3.1–11.3.4
52. C.-H. Chang, S.-C. Yan, C.-J. Sun, M.-Y. Huang, B.-A. Chen et al., *Green Laser Crystallized poly-Si thin-film Transistor and CMOS Inverter Using HfO_2-ZrO_2Superlattice Gate Insulator and Microwave Annealing for BEOL Applications*. 2023 Silicon Nanoelectronics Workshop (SNW). June 11-12, 2023, Kyoto, Japan. (IEEE, 2023), pp. 31–32
53. J.-Y. Ku, J.-M. Yu, D.-H. Wang, D.-H. Jung, J.-K. Han et al., Improved SOI FinFETs performance with low-temperature deuterium annealing. IEEE Trans. Electron Devices **70**, 3958–3962 (2023). https://doi.org/10.1109/TED.2023.3278626
54. Y. Sun, W. Qian, S. Liu, T. Dong, J. Wang et al., Unexpected phosphorus doping routine of planar silicon nanowires for integrating CMOS logics. Nanoscale **13**, 15031–15037 (2021). https://doi.org/10.1039/d1nr03014k

Publisher's Note Springer Nature remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.