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## Correction: A Valuable and Low-Budget Process Scheme of Equivalized 1 nm Technology Node Based on 2D Materials

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The original article can be found online at <https://doi.org/10.1007/s40820-025-01702-7>.

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### Correction to:

**Nano-Micro Letters (2025) 17:191**

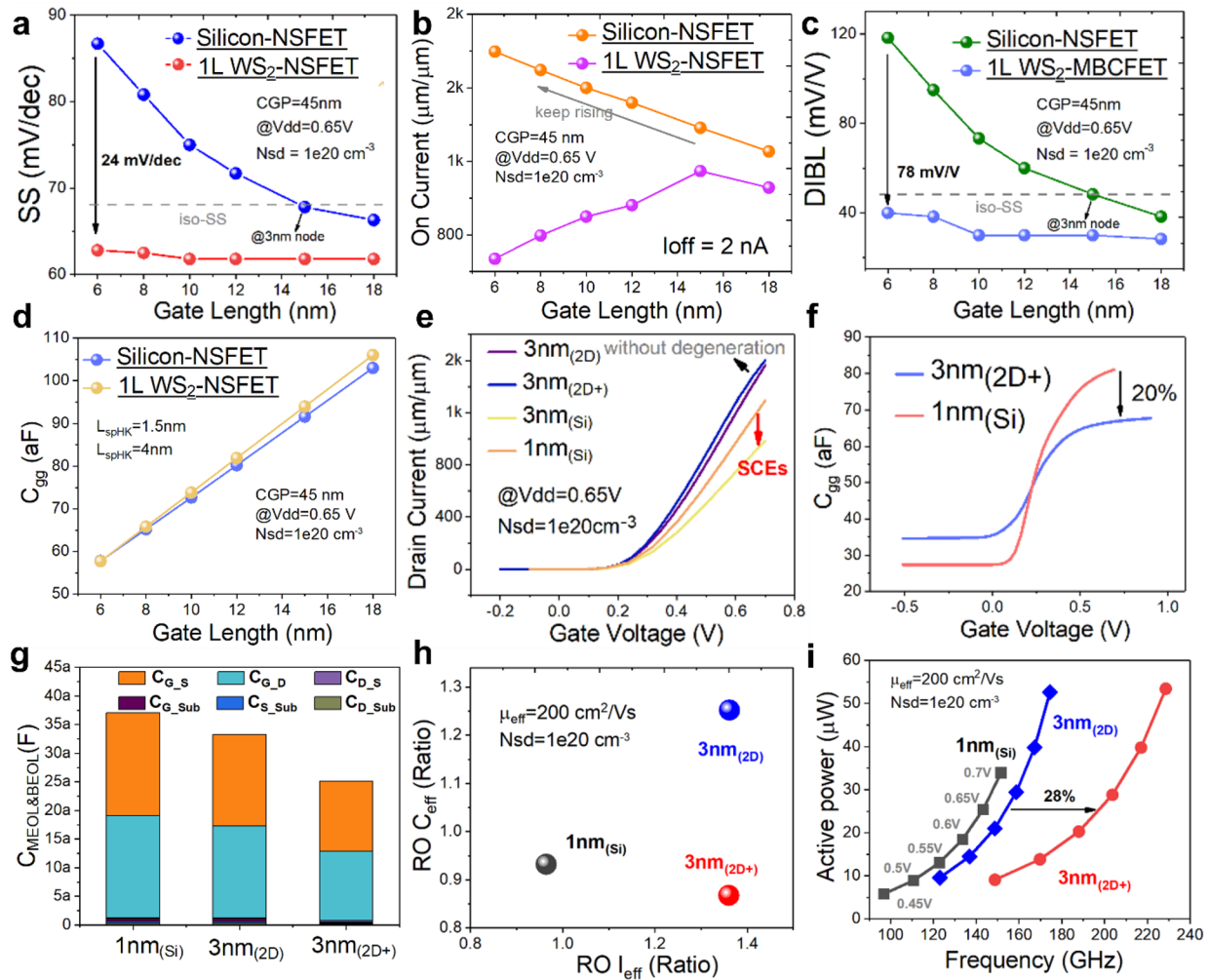
<https://doi.org/10.1007/s40820-025-01702-7>

Following the publication of the original article [1], the authors reported an error in Fig. 3(b), and the figure legend was reversed.

The correct Fig. 3 has been provided in this orrection.

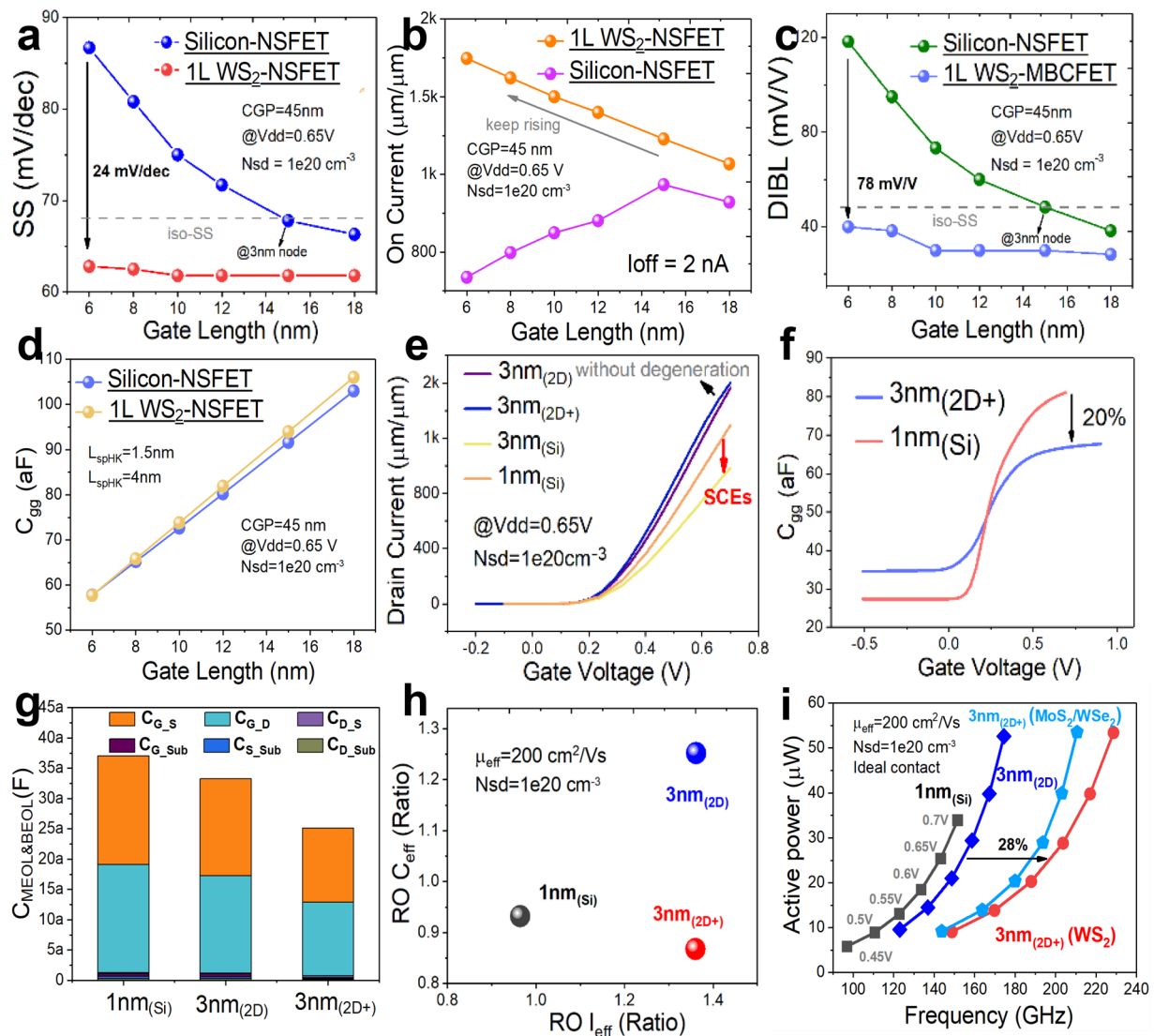


The incorrect Fig. 3 is:



**Fig. 3.** Comparison of electrical characteristics of devices at 3 nm<sub>(2D+)</sub> node, 3 nm<sub>(2D)</sub> node and 1 nm<sub>(Si)</sub> node, with fixed CGP of 45 nm and  $L_G$  shrinking from 18 to 6 nm for Si-NSFETs and WS<sub>2</sub> NSFETs. **a** SS variation, the SS of Si-NSFETs degrades drastically when the  $L_G$  is smaller than 12 nm, and **b**  $I_{ON}$  variation, thanks to the smaller feature length of 2D materials, the  $I_{ON}$  of WS<sub>2</sub> NSFETs continues to increase even with the  $L_G$  scaled to 6 nm, while the  $I_{ON}$  of Si-NSFETs degrades continuously when the  $L_G$  is reduced to 6 nm; **c** DIBL variation, which follows a similar trend to that of SS; **d**  $C_{gg}$  variations, with EOT and gate size being the main influences on  $C_{gg}$ ; **e** Linear transfer characteristics corresponding to four devices, at 3 nm<sub>(2D)</sub>, 3 nm<sub>(2D+)</sub>, 3 nm<sub>(Si)</sub> and 1 nm<sub>(Si)</sub>; **f**  $C_{gg}$ - $V_{GS}$  relationship for 3 nm<sub>(2D+)</sub> and 1 nm<sub>(Si)</sub> counterparts, which is reduced by 20% for the 3 nm<sub>(2D+)</sub> due to shortened  $L_G$ ; **g**  $C_{MEOL\&BEOL}$  comparison with middle end of line (MEOL) and back end of line (BEOL) parasitic capacitances; **h** Comparison of equivalent capacitances and equivalent currents extracted from RO circuits; and **i** Power-frequency comparison of RO circuits

The correct Fig. 3 is:



**Fig. 3.** Comparison of electrical characteristics of devices at 3 nm<sub>(2D+)</sub> node, 3 nm<sub>(2D)</sub> node and 1 nm<sub>(Si)</sub> node, with fixed CGP of 45 nm and  $L_G$  shrinking from 18 to 6 nm for Si-NSFETs and WS<sub>2</sub> NSFETs. **a** SS variation, the SS of Si-NSFETs degrades drastically when the  $L_G$  is smaller than 12 nm, and **b**  $I_{ON}$  variation, thanks to the smaller feature length of 2D materials, the  $I_{ON}$  of WS<sub>2</sub> NSFETs continues to increase even with the  $L_G$  scaled to 6 nm, while the  $I_{ON}$  of Si-NSFETs degrades continuously when the  $L_G$  is reduced to 6 nm; **c** DIBL variation, which follows a similar trend to that of SS; **d**  $C_{gg}$  variations, with EOT and gate size being the main influences on  $C_{gg}$ ; **e** Linear transfer characteristics corresponding to four devices, at 3 nm<sub>(2D)</sub>, 3 nm<sub>(2D+)</sub>, 3 nm<sub>(Si)</sub> and 1 nm<sub>(Si)</sub>; **f**  $C_{gg}$ - $V_{GS}$  relationship for 3 nm<sub>(2D+)</sub> and 1 nm<sub>(Si)</sub> counterparts, which is reduced by 20% for the 3 nm<sub>(2D+)</sub> due to shortened  $L_G$ ; **g**  $C_{MEOL\&BEOL}$  comparison with middle end of line (MEOL) and back end of line (BEOL) parasitic capacitances; **h** Comparison of equivalent capacitances and equivalent currents extracted from RO circuits; and **i** Power-frequency comparison of RO circuits

The original article [1] has been corrected.

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## References

1. Y. Shen, Z. Zhang, Z. Yao et al., A Valuable and Low-Budget Process Scheme of Equivalized 1 nm Technology Node Based on 2D Materials. *Nano-Micro Lett.* **17**, 191 (2025). <https://doi.org/10.1007/s40820-025-01702-7>