Nano-Micro Letters
e-ISSN 2150-5551
CN 31-2103/TB
CORRECTION
https://doi.org/10.1007/s40820-025-01747-8

Cite as
Nano-Micro Lett.
(2025) 17:293

Correction: A Valuable and Low-Budget Process Scheme of Equivalized 1 nm Technology Node Based on 2D Materials

Yang Shen[1], Zhejia Zhang[3], Zhujun Yao[2], Mengge Jin[1], Jintian Gao[2], Yuhan Zhao[2], Wenzhong Bao[3,4] ✉, Yabin Sun[1] ✉, He Tian[2] ✉

The original article can be found online at https://doi.org/10.1007/s40820-025-01702-7.

✉ Wenzhong Bao, baowz@fudan.edu.cn; Yabin Sun, ybsun@cee.ecnu.edu.cn; He Tian, tianhe88@tsinghua.edu.cn
[1] College of Integrated Circuit Science and Engineering, Shanghai Key Laboratory of Multidimensional Information Processing, East China Normal University, Shanghai 200241, People's Republic of China
[2] Institute of Microelectronics and Beijing National Research Center for Information Science and Technology (BNRist), Tsinghua University, Beijing 100084, People's Republic of China
[3] State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University, Shanghai 200433, People's Republic of China
[4] Shaoxin Laboratory, Shaoxing 312000, People's Republic of China

Correction to:
Nano-Micro Letters (2025) 17:191
https://doi.org/10.1007/s40820-025-01702-7

Following the publication of the original article [1], the authors reported an error in Fig. 3(b), and the figure legend was reversed.

The correct Fig. 3 has been provided in this orrection.

Published online: 12 June 2025

The incorrect Fig. 3 is:

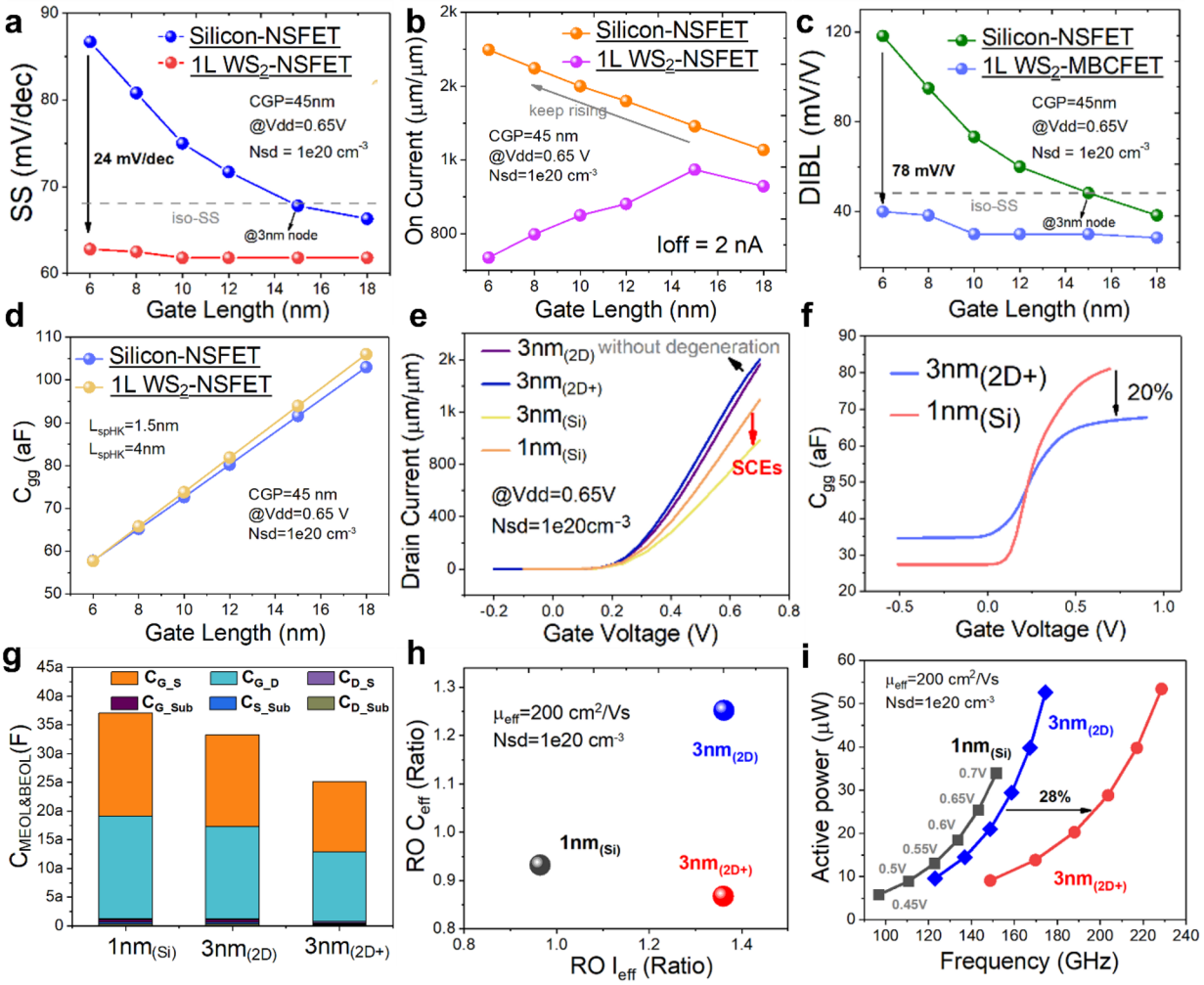

Fig. 3. Comparison of electrical characteristics of devices at 3 $nm_{(2D+)}$ node, 3 $nm_{(2D)}$ node and 1 $nm_{(Si)}$ node, with fixed CGP of 45 nm and L_G shrinking from 18 to 6 nm for Si-NSFETs and WS_2 NSFETs. **a** SS variation, the SS of Si-NSFETs degrades drastically when the L_G is smaller than 12 nm, and **b** I_{ON} variation, thanks to the smaller feature length of 2D materials, the I_{ON} of WS_2 NSFETs continues to increase even with the L_G scaled to 6 nm, while the I_{ON} of Si-NSFETs degrades continuously when the L_G is reduced to 6 nm; **c** DIBL variation, which follows a similar trend to that of SS; **d** C_{gg} variations, with EOT and gate size being the main influences on C_{gg}; **e** Linear transfer characteristics corresponding to four devices, at 3 $nm_{(2D)}$, 3 $nm_{(2D+)}$, 3 $nm_{(Si)}$ and 1 $nm_{(Si)}$; **f** C_{gg}-V_{GS} relationship for 3 $nm_{(2D+)}$ and 1 $nm_{(Si)}$ counterparts, which is reduced by 20% for the 3 $nm_{(2D+)}$ due to shortened L_G; **g** $C_{MEOL\&BEOL}$ comparison with middle end of line (MEOL) and back end of line (BEOL) parasitic capacitances; **h** Comparison of equivalent capacitances and equivalent currents extracted from RO circuits; and **i** Power–frequency comparison of RO circuits

https://doi.org/10.1007/s40820-025-01747-8

The correct Fig. 3 is:

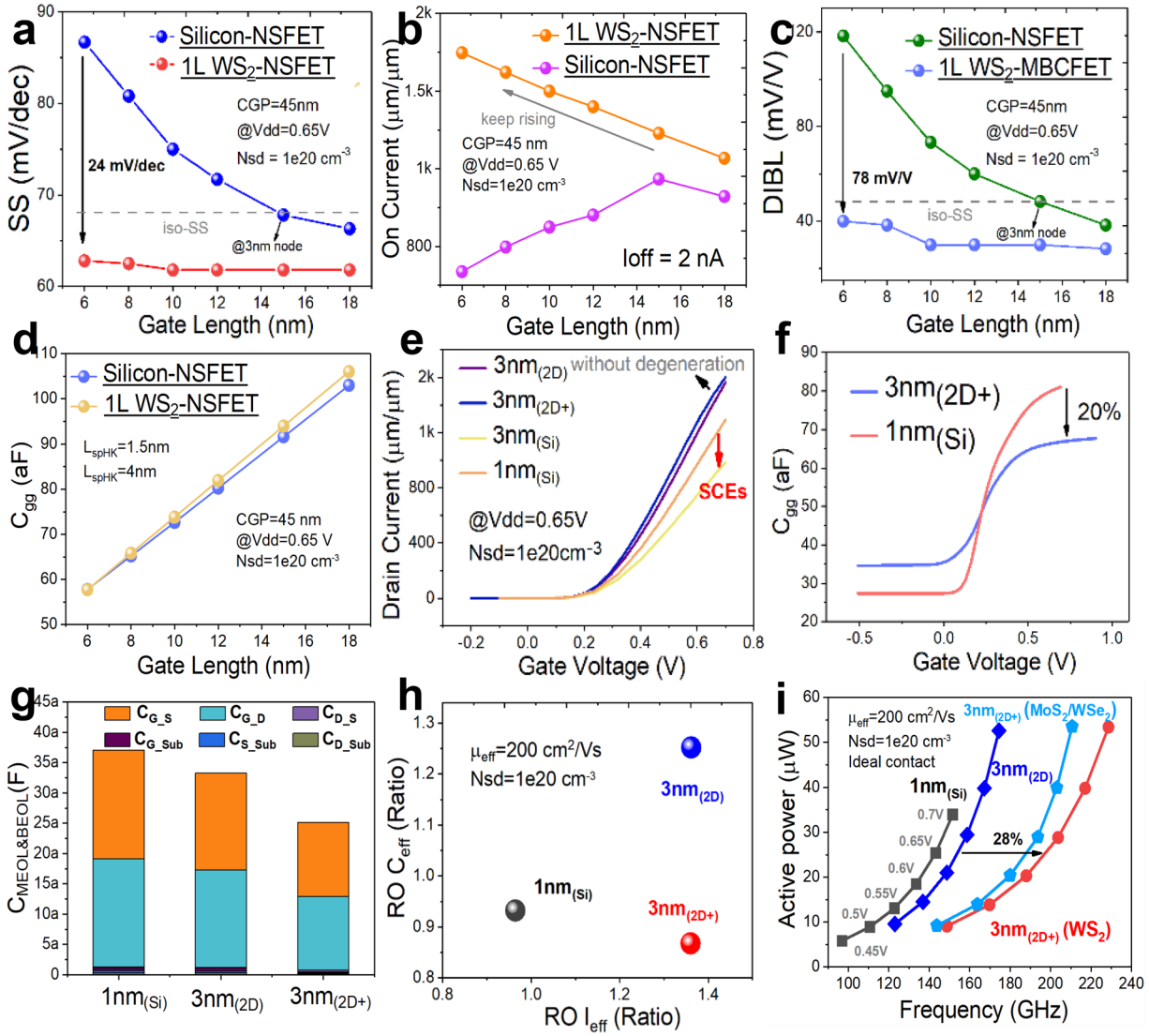

Fig. 3. Comparison of electrical characteristics of devices at 3 $nm_{(2D+)}$ node, 3 $nm_{(2D)}$ node and 1 $nm_{(Si)}$ node, with fixed CGP of 45 nm and L_G shrinking from 18 to 6 nm for Si-NSFETs and WS_2 NSFETs. **a** SS variation, the SS of Si-NSFETs degrades drastically when the L_G is smaller than 12 nm, and **b** I_{ON} variation, thanks to the smaller feature length of 2D materials, the I_{ON} of WS_2 NSFETs continues to increase even with the L_G scaled to 6 nm, while the I_{ON} of Si-NSFETs degrades continuously when the L_G is reduced to 6 nm; **c** DIBL variation, which follows a similar trend to that of SS; **d** C_{gg} variations, with EOT and gate size being the main influences on C_{gg}; **e** Linear transfer characteristics corresponding to four devices, at 3 $nm_{(2D)}$, 3 $nm_{(2D+)}$, 3 $nm_{(Si)}$ and 1 $nm_{(Si)}$; **f** C_{gg}-V_{GS} relationship for 3 $nm_{(2D+)}$ and 1 $nm_{(Si)}$ counterparts, which is reduced by 20% for the 3 $nm_{(2D+)}$ due to shortened L_G; **g** $C_{MEOL\&BEOL}$ comparison with middle end of line (MEOL) and back end of line (BEOL) parasitic capacitances; **h** Comparison of equivalent capacitances and equivalent currents extracted from RO circuits; and **i** Power–frequency comparison of RO circuits

The original article [1] has been corrected.

References

1. Y. Shen, Z. Zhang, Z. Yao et al., A Valuable and Low-Budget Process Scheme of Equivalized 1 nm Technology Node Based on 2D Materials. Nano-Micro Lett. **17**, 191 (2025). https://doi.org/10.1007/s40820-025-01702-7