

Two-Dimensional Transition Metal Dichalcogenides and Their Charge Carrier Mobilities in Field-Effect Transistors

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Abstract Two-dimensional (2D) materials have attracted extensive interest due to their excellent electrical, thermal, mechanical, and optical properties. Graphene has been one of the most explored 2D materials. However, its zero band gap has limited its applications in electronic devices. Transition metal dichalcogenide (TMDC), another kind of 2D material, has a nonzero direct band gap (same charge carrier momentum in valence and conduction band) at monolayer state, promising for the efficient switching devices (e.g., field-effect transistors). This review mainly focuses on the recent advances in charge carrier mobility and the challenges to achieve high mobility in the electronic devices based on 2D-TMDC materials and also includes an introduction of 2D materials along with the synthesis techniques. Finally, this review describes the possible methodology and future prospective to enhance the charge carrier mobility for electronic devices.

Keywords 2D materials · TMDC layers · Charge carrier mobility · Field-effect transistor · Heterostructure · Charge carrier scattering

1 Introduction

Discovery of graphene has diverted the interest of researchers toward a new family of nanomaterials known as 2D materials. Unique properties of 2D materials have been widely utilized for diverse applications such as catalysis, supercapacitors, energy storage devices, and high-performance sensors. Besides graphene, transition metal dichalcogenides (TMDCs) and layered oxide materials are also parts of 2D materials family. 2D materials have shown promising properties in the application of electronic devices [1, 2]. Semiconductor behavior of 2D materials (e.g., MoS₂) makes them promising materials for field-effect transistors (FETs). The FET fabricated from 2D materials will not only exhibit improved performance, in

terms of fast processing rate and low power consumption, but also allow further reduction in device dimensions which is the need for the fabrication of next-generation electronic devices. In recent years, many efforts have been made to review the research on the synthesis, characterization of single- and few-layered 2D materials including their electronic, magnetic, optical and mechanical properties as well as applications [3–9]. Furthermore, some reviews focused on the utilization of 2D materials in a variety of applications such as flexible and transparent electronic, optoelectronic devices [10–15], energy conversion and storage [16, 17], hydrogen generation [18], and gas sensors [19]. It is well known that most 2D layered materials exist in a bulk state. These materials have layered structure and weak interlayer van der Waals force holding these layers together. Layered structure makes it possible to achieve monolayer or a few layers of 2D materials by mechanical exfoliation. On the other hand, in-plane atoms are connected with strong covalent bonds [1, 20]. Hence, monolayer 2D materials possess two-dimensional features

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in the lateral x - y direction and quantum confinement in the third dimension, which makes these materials unique from their bulk counterparts. One of the features is high carrier mobility, which is essential for high-speed transistors. For a high-performance transistor, good ohmic contact, higher carrier mobility, and appropriate band gap (~ 1 eV) are the basic requirements [12]. Graphene, the most extensively studied 2D material, has exhibited very high carrier mobility ($\sim 2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) at the temperature of 5 K [21]. However, it is not suitable for logic applications due to its zero band gap, resulting in very small on/off ratio (<10) at ambient temperature. In order to improve its on/off ratio, the opening of band gap has been proposed. However, engineering the band gap up to ~ 400 meV will lead to a decrease in the mobility to less than $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. Similarly, p-type device, based on the graphene nanoribbons, demonstrates a band gap opening due to the various edge (armchair or zigzag) structures resulting in very high on/off ratio of $\sim 10^6$ and extremely low charge carrier mobility of ~ 100 – $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, as compared to other members of graphene family. However, these devices have shown the subthreshold slope (SS) of ~ 210 mV per decade, which is not desirable and ideal. It needs to be ~ 60 mV per decade at room temperature [22]. In contrast to graphene, TMDCs, such as MoS_2 (1.8 eV), WS_2 (2.1 eV), MoTe_2 (1.1 eV), and WSe_2 (1.7 eV), have desirable band gap [12, 23, 24]. MoS_2 is one of the most promising materials for logic devices such as metal–oxide–semiconductor field-effect transistors (MOSFETs) due to its tunable band gap, high on/off ratio and relatively cheap price. The band gap of monolayer MoS_2 has been reported to be 1.8 eV earlier. However, recent work demonstrates it has a direct band gap of 2.5 eV, while its bulk counterpart has an indirect band gap of 1.2 eV [25–28]. Being a relatively large band gap material, experimentally, MoS_2 only shows low carrier mobility of $\sim 1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ without high- k dielectric gate material [29], whereas the mobility can reach $\sim 150 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at 300 K with HfO_2 as the top-gate layer [30–33]. In addition, theoretical calculation based on density functional theory has indicated that the mobility of MoS_2 can reach $400 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [34] at room temperature. More recently, another type of 2D material, black phosphorus, has been predicted to have a hole mobility of 10,000–26,000 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [35], and experimentally, a mobility of 1000 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ has been achieved [36], showing very promising potential for electronic devices [37].

In this review, we mainly focus on the recent development of the charge carrier mobility in 2D TMDC materials and the challenges for achieving high mobility as well as high current on/off ratio simultaneously, which are essential for 2D TMDC-based electronic devices. We also give an introduction of 2D materials (including TMDCs) and their synthesis using different approaches. Finally, this

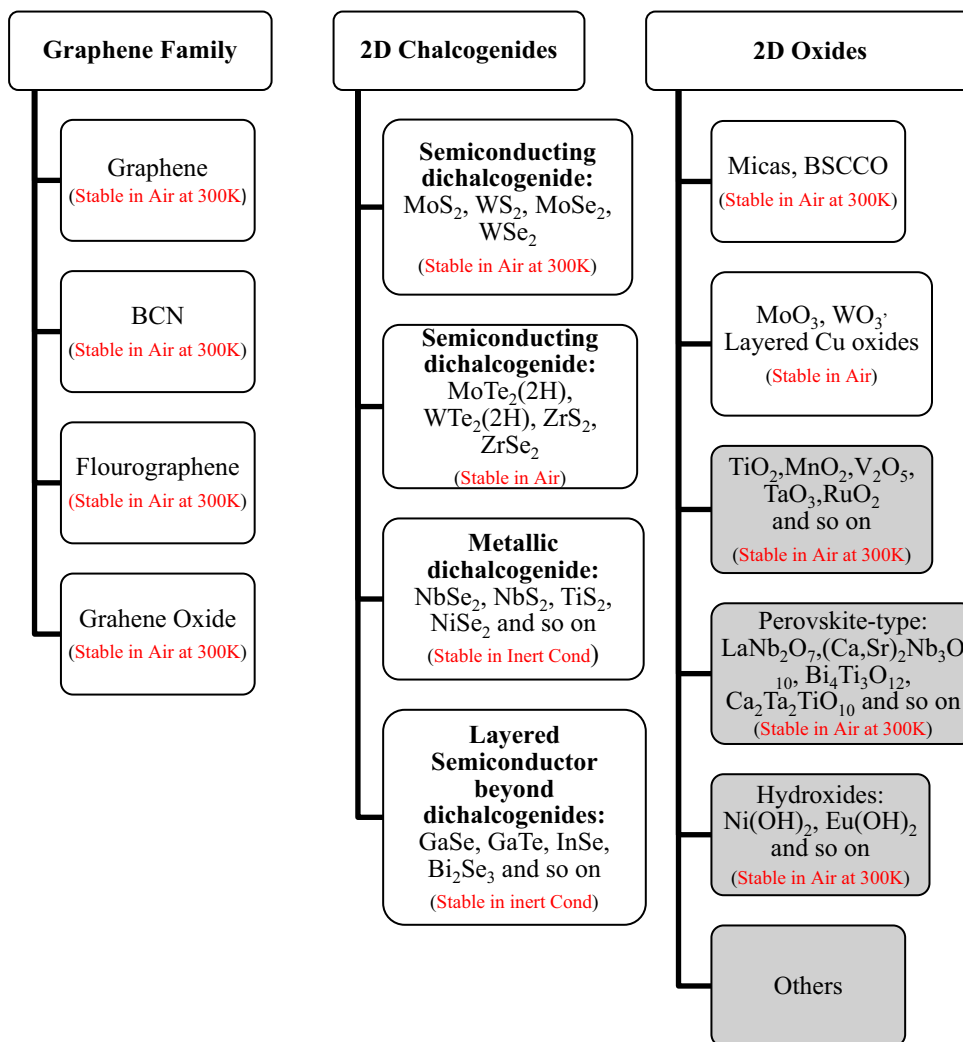
review describes the possible methodology and future prospective to enhance the charge carrier mobility for electronic devices.

2 2D Materials

Recent advancements in science and technology have unveiled the new prospects and put the mankind on the foundation of the newly developed field named as nanotechnology. This technology has enabled us to conduct research and work in the domain up to nanometer scale, resulting in the technologies which were never possible earlier. These technologies include cancer therapy based on nanoparticles, nanocomposites and innovative medicine, high-performance nanoelectronics, and highly sensitive sensors [38–41]. Evolution of nanotechnology has also introduced the distinguished class of low-dimensional systems such as zero-dimensional (0D, i.e., nanoparticles), one-dimensional (1D, i.e., nanowires), two-dimensional (2D, i.e., graphene), and three-dimensional (3D, i.e., bulk materials). The low-dimensional system plays an important role in classifying the nanomaterials, as the dimension of the material will not only define the atomic structure but also the properties of the nanomaterials [42].

In 2004, Geim and Novoselov [43] obtained a layered structure by mechanical exfoliation using scotch tape, which is later called graphene. The discovery of graphene has opened a new area of research—2D materials. These materials have shown many excellent properties widely used for energy, sensors, catalysis, electronic devices, spintronic devices as well as biomedical applications [3]. The discovery of graphene has triggered the research interest toward other two-dimensional materials, such as silicene, black phosphorus, transition metal dichalcogenides (TMDCs), and layered oxide materials. One of the most important features of these 2D materials is the high mobility of the carriers due to their quantum confinement in the third dimension, which is promising for the applications of electronic devices, such as transistors [1, 2].

As described previously, graphene has exhibited very high carrier mobility [21]. However, it is unsuitable for the applications in transistors since materials used to make transistors have to be able to switch current on and off to create logic circuits. Different from graphene, MoS_2 , one of the TMDCs, has a direct band gap in monolayer structure, which makes it possible to tune the carriers transport in an electronic device, thus realizing the device functions. Among the 2D materials, currently, TMDCs have attracted more and more interest due to their natural abundance and unique/diverse properties. The generalized chemical formula for TMDCs is MX_2 , where M represents the transition metal (typically Ti, Zr, Hf, Mo, W, Nb, Re, V, and Ni)

Table 1 2D materials family [1, 9, 20, 29, 42, 66–70]

of group 4–10 [26, 44] and X is a chalcogen (S, Te, and Se) [45]. Presently, more than 40 different TMDCs combinations have been reported [28, 46–48] and they have shown distinctive properties. In TMDCs, M (transition metal) layer sandwiched between two (02) X (chalcogen) atomic layers. Different atomic arrangements can generate the octahedral (tetragonal, T) and trigonal prismatic (hexagonal, H) structure of the 2D TMDCs. In H-phase TMDC, hexagonal symmetry can be observed from a top view and X-M-X arrangement is considered to be the monolayer, in which each M atom is covalently bonded to the six X atoms [49], whereas T-phase has a trigonal arrangement of the chalcogen (X) atoms on the top and shows the hexagonal structure of chalcogen atoms from a top view [50]. Among both, the 2H phase of 2D TMDCs is stable in air [51]. The stability of mono or few layer TMDC is of the vital importance due to its layer dependent properties [52]. The

conductivity of 1T MoS₂ phase is 10⁷ times better than 2H MoS₂ phase [53]. Due to the tunable band gap, quantum confinement and surface effects, monolayer 2D TMDCs (MoS₂, WS₂) exhibit strong photoluminescence (PL) and large exciton binding energy [54]. Besides the TMDCs, two-dimensional oxides have also been extensively investigated. Two-dimensional oxides include micas and layered oxides, such as MoO₃ [55] and WO₃ (micas) [56], TiO₂, MnO₂, V₂O₅, TaO₃, and RuO₂ [28, 57–61]. These oxides have also shown very promising properties for a variety of applications.

The family members of 2D graphene, TMDCs, and oxide materials are shown in Table 1. Gray color shows the monolayer fabricated by exfoliation. These 2D materials can be categorized in several ways in terms of their electrical, mechanical and transport properties, as they possess excellent and unique mechanical, thermal, optical, and

electronic properties [62–65] which have the potential to replace current silicon-based semiconductor devices in the future.

2.1 Classification of 2D Materials

For a better understanding of properties and its applications, 2D materials can be categorized in following three classes.

2.1.1 Layered van der Waals Solids

The most common type of 2D material is the layered van der Waals solid which has strong in-plane covalent or ionic bond and weak interlayer van der Waals bonding. This weak out-of-plane bonding allows the extraction of mono or few layers of 2D materials from their bulk counterpart through mechanical or liquid exfoliation. The dimensions of these materials in the lateral direction are up to a few micrometers and are less than 1 nm in thickness. TMDCs, especially MoS₂, MoSe₂, and WS₂, are the well-studied materials. Besides those materials described afore, presently there are more than 40 different combinations of 2D layered TMDCs (X-M-X) reported [46, 47]. The transition metal, presenting in TMDCs, occupies trigonal prismatic or octahedral coordinates and forms the hexagonal structure [71]. Besides TMDCs, there are some other members of layered van der Waals solids as well, such as Sb₂Te₃ [72], vanadium oxide [73], and h-BN [74] etc.

2.1.2 Layered Ionic Solids

In this type of 2D materials, charged polyhedral layer is present between two layers of halide or hydroxide layers and these layers are held together via electrostatic force between them. Ion exchange liquid exfoliation or ion intercalation can be used to exfoliate the mono or few layered 2D materials. Typical layered ionic materials exfoliated from ion exchange methods are KCa₂Nb₃O₁₀ [75], RbLnTa₂O₇, K₂Ln₂Ti₃O₁₀ [75], and La_{0.9}Eu_{0.05}Nb₂O₇ [76].

2.1.3 Surface-Assisted Non-Layered Solids

This type of 2D nanostructure materials is synthesized by making the layers artificially stacked on a substrate with arbitrary angles [77]. The methods to synthesize these materials include epitaxial growth and chemical vapor deposition. Silicene is a typical example of this class. However, its instability at ambient condition is the real challenge to make it feasible for the application in electronic applications [78, 79]. Ge/Ag (100) and Ag(111) [80, 81], TiO₂ [82] and MgO/Mo (001) [83], and Al₂O₃/

SiO₂ [84] are the examples of surface-assisted non-layered solids.

2.2 Synthesis Techniques for 2D Materials

2D materials can be synthesized by following techniques:

2.2.1 Micromechanical Exfoliation

This process was first discovered by Geim and Novoselov in 2004 [43], and the monolayer graphene was achieved [85], in which parent bulk material was peeled off by micromechanical force of the scotch tape and placed on the surface of the photoresist. This cleavage is possible due to the weak interlayer van der Waals forces. Monolayers of NbSe₂ [29], MoS₂ [29, 86], and WS₂ [87] are some of the examples obtained by this process besides graphene. Despite being the fast and cost-effective process, micromechanical exfoliation is not an industrial-level production of monolayer materials since most of the flakes are smaller than 20 μm in diameter. In addition to the monolayer, a few layers or very thick layers can also be achieved at the same time. On the other hand, because of the absence of chemical interaction, monolayer obtained by this process is highly crystalline and its structural integrity can be maintained. This monolayer has shown good stability at ambient conditions up to the months' exposure [29, 88].

2.2.2 Liquid Exfoliation

In contrast to mechanical exfoliation, which is a low yield method, liquid exfoliation is capable of producing the mono or few layers of 2D materials at a large scale. Mono or few layers of Bi₂Te₃, TaSe₂, MoSe₂, MoTe₂, BN, WS₂, and MoS₂ can be easily obtained by this method [1, 89–91]. This method can be categorized into four different forms such as oxidation, intercalation, ion exchange, and ultrasonic cleavage.

Graphene oxide can be synthesized with an oxidation method by treating graphite flakes with potassium permanganate or potassium chlorate and nitric acid or sulfuric acid or their mixture [92–94]. The addition and dispersion of epoxide functional groups or –OH in a polar solvent and subsequent sonication result in exfoliated graphene oxide. This method is also known as Hummers method or modified Hummer method [94, 95]. An oxidative form of liquid exfoliation is most suitable for layered materials possessing low reduction potential.

The intercalation technique is equally applicable to TMDCs and graphene. In this method, interlayer force decreases due to the intercalation of ionic or organic

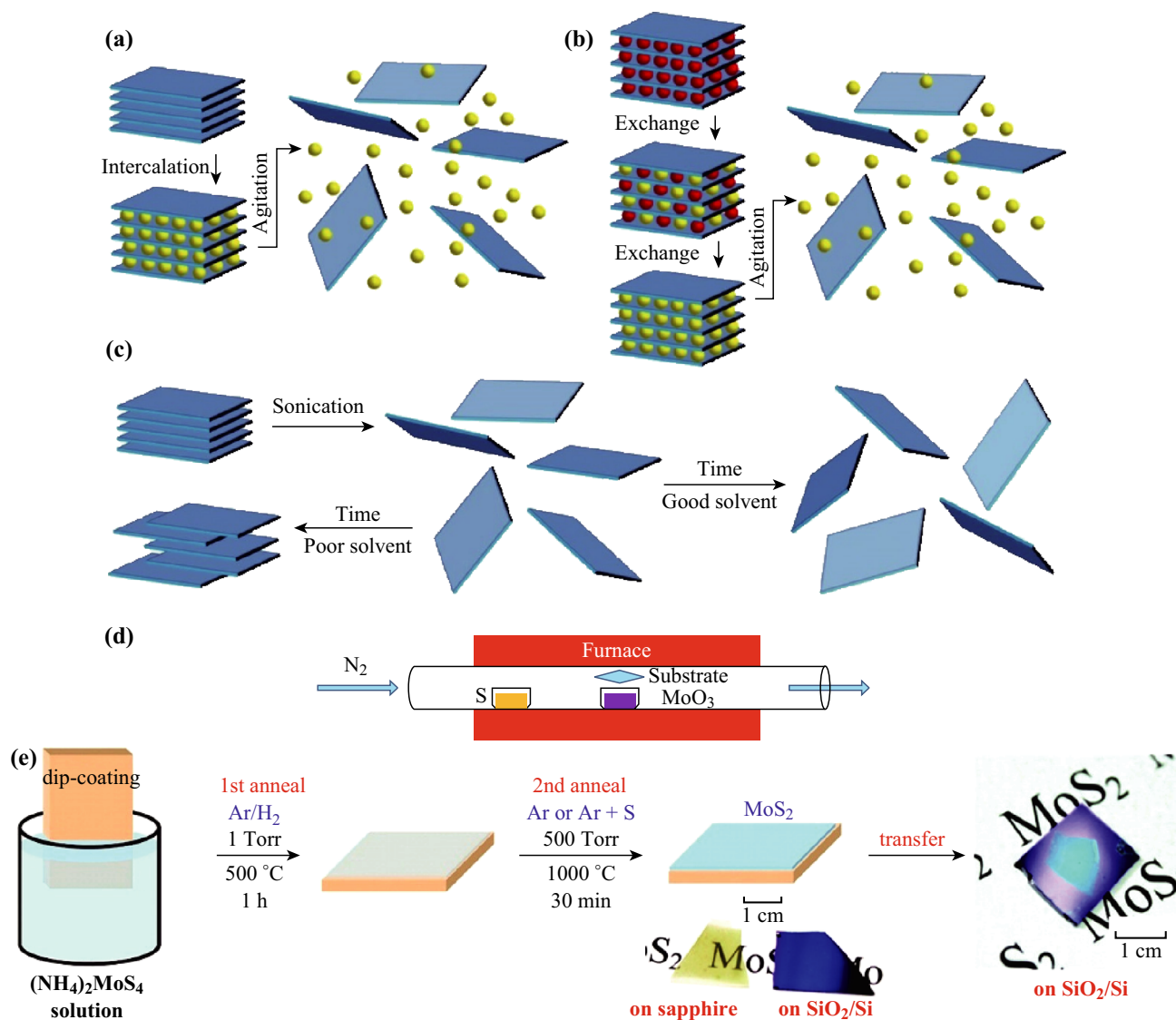


Fig. 1 Schematic representation of the variation in liquid exfoliation process: **a** intercalation, **b** ion exchange, and **c** ultrasonic exfoliation. **a–c** Reprinted from Ref. [98] with permission from Copyright 2013, AAAS. **d** Schematic representation of the CVD process. **e** Schematic representation of large-area MoS₂ nanosheet synthesis via dip and anneal technique. Reprinted with permission from Ref. [101], Copyright 2012, American Chemical Society

molecules, which results in a decrease in energy required for exfoliation [96, 97].

Another technique to obtain a single- or few-layered 2D material by liquid exfoliation is ultrasonic cleavage. In this technique, parent bulk material consisting of layers with weak interlayer bonding is ultrasonicated for 1–3 h after dispersion in a suitable solvent. In this process, cavitation bubbles are developed in the solvent due to high-energy ultrasonic waves [98]. The exfoliation of layers is possible due to the pressure released by the burst of cavitation bubbles. Subsequently, centrifugation is applied to separate the crystals. Figure 1a–c represents the schematic diagram of the above-mentioned forms of liquid exfoliation. Due to the complexity and destructive nature of liquid exfoliation

method, layered 2D nanostructure material cleaved by mechanical exfoliation remains the favorite choice in the research community [9].

2.2.3 Chemical Vapor Deposition (CVD)

CVD is known as a bottom-up technique allowing the synthesis of 2D layers at a large scale with uniform thickness, which is promising for optoelectronics and electronic devices. Synthesis of MoS₂ 2D nanostructured sheets by CVD on an oxidized silicon substrate is one of the recent developments. Generally, there are two ways for the fabrication of monolayer 2D materials. MoS₂ as an example, first, in a so-called two-step bottom-up technique,

a thin layer of metallic Mo is evaporated by an e-beam evaporation system. The Mo layer then reacts with sulfur vapors, generated by heating the elemental sulfur above its melting temperature. This reaction occurs at 750 °C leading to the formation of monolayered MoS₂ [99]. This method can yield MoS₂ with a thickness more than three layers. Second, a so-called one-step bottom-up technique is used for the synthesis of the atomically thick MoS₂ nanosheets. In this approach, pure S and MoO₃ powders are put in a CVD system. The mixture is heated to 650 °C. Then, the atomic layer of MoS₂ will be grown on the Si substrate, which is covered with the rGO (reduced graphene oxide) for MoS₂ layers growth. The rGO acts as a catalyst and the seed to enhance the growth of MoS₂ layers [100], as shown in Fig. 1d. By this approach, MoS₂ monolayer with a thickness of 0.72 nm has been obtained. Furthermore, large-area MoS₂ nanostructured sheets can be obtained by dip coating of (NH₄)₂MoS₄ (ammonium thiomolybdate) dissolved in DMF (dimethylformamide) on silicon or silicon dioxide substrate [100, 101]. Figure 1e shows the pictorial representation of this approach. After the (NH₄)₂MoS₄ solution is dipped onto the substrate, the substrate is annealed under Ar/H₂ atmosphere at 500 °C for 1 h. Then, the substrate is subsequently performed the second annealing at 1000 °C for 30 min under Ar or Ar⁺S atmosphere [101]. MoS₂ 2D layer nanosheets are then obtained. X-ray diffraction (XRD), atomic force microscope (AFM), and transmission electron microscopy (TEM) analysis indicate that the layers grow and overlap each other without interlayer chemical bonding. Besides MoS₂, other 2D materials such as TiS₂ [102], VSe₂ [103], WSe₂ [104], WS₂ [105], and MoSe₂ [106] were also produced using CVD technique.

In addition, thermally decomposed (BN)₃H₆ (borazine) or (ClBNH)₃ B-trichloroborazine can be used to fabricate the layered BN on transferred metal surfaces, e.g., Rh, Pd, Ru, Ni, and Pt, through an ultrahigh-vacuum CVD technique at a temperature above 700 °C [107–109].

2.2.4 Van der Waals Epitaxial Growth on a Substrate

This technique is similar to the CVD method. The only difference is that the substrate used in van der Waals epitaxial method also acts as a seed crystal. A variety of layered 2D nanostructured sheets can be synthesized by this method, such as MoS₂, GaSe, h-BN, and hexagonal Si [107, 110–112].

Hexagonal Si is one of the examples achieved by this method. Si superstructures were deposited on Ag (001) substrate by heating the Si single crystal in ultrahigh vacuum using direct current. However, low-energy electron diffraction (LEED), scanning tunneling microscopy (STM), and XRD analysis indicated that there are two

kinds of superstructures in the deposited layer [113]. Initially, a monolayer of Si nanostructure p (3 × 3) was formed. Subsequently, complex structure p (7 × 4) was observed. Direct current deposition formed the atomic thick Si nanoribbons on Ag (110) substrate. The atoms in Si nanoribbons were arranged in a honeycomb structure [114, 115]. Minor distortion was produced by the Si nanostructure on Ag substrate. Similar to that of hexagonal Si, monolayered Ge was also obtained by van der Waals epitaxial growth method on Ag (110) and Ag (111) substrates [116], whereas, due to the high solubility of Ge in Ag, the tetramers structure of Ge on Ag substrate leads to a larger distortion than that of Si [116].

Large-area 2D nanostructured materials, which are difficult to obtain via liquid and mechanical exfoliation, may be synthesized by van der Waals epitaxial growth method. However, the structure and properties of the 2D materials fabricated by this method are critically dependent on the orientation of the substrate and its chemistry. Moreover, in respect of future applications, this method is not suitable for the commercial applications, as it requires high vacuum and high temperature leading to high cost.

2.2.5 Hydrothermal Synthesis

Hydrothermal method is defined as the crystallization of substance from organic or aqueous solution at high vapor pressure and temperature. Due to extreme conditions, this method is only suitable for those precursors which can withstand these harsh conditions. 2D layered nanostructured materials have been successfully synthesized by this approach. Single-layered MoSe₂ and MoS₂ nanostructures were obtained through chemical reaction of Se/S with (NH₄)₆Mo₇O₂₄·4H₂O (ammonium molybdate) in hydrazine monohydrate solution at a temperature of 150–180 °C for 48 h [117]. Furthermore, the single-step solvothermal reaction of hydrazine and (NH₄)₂MoS₄ on GO, in C₃H₇NO (N, N-dimethylformamide) solution has produced the 3 to 10 layered MoS₂ flakes [118].

Besides the synthesis of the MoS₂ mono and few layered 2D nanostructures, other 2D materials have also been fabricated by the hydrothermal approach. Transition metal (groups IV and V) chalcogenides 2D nanostructures have been synthesized from metal chloride in oleylamine [119]. In this process, chalcogen sources such as elemental selenium, sulfur, or compound CS₂ are employed. When sulfur is used as the source, irregular shape and poor crystallinity of TMDC is obtained which is mainly due to the highly reactive radical formation. In contrast, better crystallinity can be achieved when using elemental Se as the source [119]. When CS₂ is employed initially, H₂S is generated followed by its reaction with metal precursor, resulting in the formation of metal disulfide 2D layered crystals with

variable lateral size in (001) plane. This growth is due to the low surface energy of this particular plane compared to (010) and (100) planes.

Besides the synthesis of TMDCs, this method has a potential to synthesize the 2D nanostructured sheets of hydroxides or metal oxides such as nanoribbons of VO_2 , which can be obtained by hydrothermal reduction in V_2O_5 in the presence of GOIt and is promising for applications in Li-ion batteries as a cathode [73]. Characterization techniques such as STM, X-ray photoelectron spectroscopy (XPS), and high-resolution transmission electron microscopy (HRTEM) have shown good composition control and crystal structure of 2D nanostructure materials synthesized by this approach.

2.3 Properties and Applications of 2D Materials

The layered materials in which one dimension is restricted to a single layer are called 2D materials. In 2D materials, the increment in excitation energy leads to an increase in the density of states [120], resulting in different properties with different sizes and shapes of the quantum confined 2D materials. 2D materials exhibit dissimilar properties than their bulk counterpart and demonstrate the shape- and size-dependent properties, which make them suitable for a variety of nanoapplications [121].

2D layered nanomaterials have electron confinement and the layers are in close contact by van der Waals force, which results in a minimization of the interlayer interaction. Large surface-to-volume ratio allows altering the properties through surface treatments such as chemical functionalization [122]. Moreover, 2D materials can also be synthesized as dispersed nanoflakes, which can retain their properties similar to the monolayers. In addition, these nanoflakes can be mixed with other materials to form nanocomposites, which have been widely used for energy applications [89, 123, 124]. Highly conductive nature coupled with large surface area, excellent chemical stability, and flexibility make 2D materials as suitable candidates for the applications of energy storage and conversion [16]. 2D materials can also be utilized in fuel cells due to their photocatalytic properties [125]. Moreover, anodes made from graphene have shown enhanced cyclic lithium storage capacity (specific capacity of 460 mAh g^{-1}), which can be utilized in the flexible battery devices [126–128]. 2D materials have also shown promising properties for supercapacitors. Recently, supercapacitors made from multilayered reduced graphene oxide have demonstrated a high specific capacity of $394 \mu\text{F cm}^{-2}$ [129].

Graphene has given rise to high charge carrier mobility, chiral properties of the mobile carriers, and high thermal conductivity [3]. Charge carriers in graphene can be well described by Dirac equation rather than the Schrödinger

equation [130, 131]. It is well known that graphene is a gapless semiconductor. High symmetry of honeycomb lattice protects the zero gap of single-layer crystal. However, the band gap of bilayer graphene can reach up to 250 meV by the application of a transverse electric field and the band gap is tunable by an electric field [132]. Besides electric field effect, strain can also alter the low-energy band structure of layered 2D materials. For example, the band gap of a single- and bilayered MoS_2 decreases linearly with strain at the rate of ~ 45 and $\sim 120 \text{ meV/\%}$, respectively [133, 134]. Furthermore, magnetic field also has a strong impact on electronic properties of 2D materials [43, 135, 136]. Charge carrier sign of 2D nanostructure materials can be modified by the application of electrical field allowing its utilization in high-mobility p–n junction transistors and complementary metal oxide semiconductor (CMOS) technology. Defect-free high-quality crystal up to micron scale [137] is the main reason for achieving high charge carrier mobility due to scattering free movement of electrons [138]. Therefore, 2D materials are very popular in the design of nanoelectronic devices such as field-effect transistors (FET) due to their high charge carrier mobility, high on/off current ratios, and low power consumption. FET composed of pristine graphene exhibits very high electron mobility ($200,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) [21] but lacks in on/off ratio. In contrast, some 2D materials such as MoS_2 (TMDC) exhibit variable band gap (1.2 eV, indirect to 2.5 eV, direct from bulk to a single layer) [26–28, 139]. Indirect-to-direct transition of band gap from bulk to the single-layered 2D material is due to the upshift of the indirect band gap induced by strong quantum confinement effect in a single layer [26]. This intrinsic large band gap of such single-layered 2D material gives rise to 10^8 on/off ratio and $\sim 150 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ electron mobility at 300 K for transistor application [30–33]. Furthermore, due to quantum limitations, channel thickness of $<5 \text{ nm}$ cannot be achieved in Si-based devices, as it reduces the carrier mobility significantly due to scattering generated by surface roughness [140]. Thus, two-dimensionality of TMDCs gives the advantage of dangling bonds free, fully terminated surface [13]. In comparison with Si transistors, it demonstrates 10^5 times less power consumption [30]. Similar to TMDC, 2D phosphorene has also shown promising results for transistor applications [141]. In addition, mechanical strains and electrical field both have significant influences on the band structure of 2D nanostructured materials, which makes them suitable candidates for sensor applications. High mobility results in highly sensitive conductivity (to electrostatic perturbation) of 2D materials due to the possible generation of carriers on the surface via photo (light)-effects [142]. This property makes these materials potential candidates for high-gain photodetector application such as optical communications,

optoelectronic devices, and biomedical imaging. 2D materials can also be used as the nanogenerators [6] which convert the biomechanical energy, induced by the human body motion, into the electrical signal. This property makes them promising for biosensor and body implanted device applications [6, 143]. 2D materials can absorb a large range of the electromagnetic spectrum (infrared to ultraviolet) [144] allowing their utilization in high-performance photonics and optics [145]. Atomic layer graphene can be used for ultrafast photonics application due to its wavelength independent ultrafast saturable absorption [146]. 2D topological insulators (e.g., Bi_2Se_3) have the potential to be utilized for nonlinear optics applications at high-power regime (low absorption and high nonlinear phase) [147]. Few-layered 2D TMDC materials or MoS_2 nanoplatelets possess nonlinear optical properties and can potentially be used in laser photonic devices [148]. Black phosphorus is also a promising nonlinear optical material. Thin films of black phosphorus can be used in developing ultrafast photonic devices [149]. 2D materials have very low absorbance value ($<10\%$) and high conductivity, making them suitable for flexible and transparent electronic applications such as liquid crystal devices and solar cells [150, 151].

Along with the extraordinary electrical and photonic properties, 2D materials also display excellent mechanical properties. The 2D material, such as graphene, is very flexible and has demonstrated 200 times higher breaking strength than steel [152]. Hence, it can be used to reinforce the polymers. Furthermore, its membrane can also be used in nonlinear electromechanical systems due to its extraordinary flexibility and ultrathin nature [153].

3 Field-Effect Transistors

3.1 Introduction

In general, the transistor is a device which controls the flow of the electrical charge carriers across a semiconductor material by which it is fabricated. Field-effect transistors (FETs) are the particular class of transistors in which semiconductor material is used as a channel. The current carrier density and conductivity of a semiconductor channel are controlled by an applied voltage resulted from the regulated current flow passing through it by a supply. Both ends of the channel connected to the input supply are denoted as the source and drain terminals. The terminal which is responsible for controlling the conductivity and current flow through the channel, upon the application of the potential, is known as a gate terminal, as shown in Fig. 2.

The basic principal of the FET is not new and was first described by J.E. Lilienfeld in a patent of 1925. The

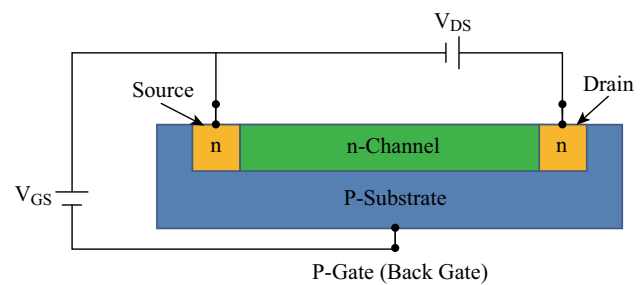


Fig. 2 Idealized N-channel junction FET

development of electronic devices was made possible after the theoretical description of the concept related to FET, given by Shockley in 1952 [154]. The general field-effect transistors can be categorized into two major classes, junction FET (JFET) and metal oxide semiconductor FET (MOSFET), also known as an insulated gate FET (IGFET), as shown in Fig. 3. In the era of 1970–1980, the invention of a MOSFET has led to the revolution of the electronic circuits and the development of the microprocessors, resulting in the powerful portable calculators and computers. FET has a variety of applications such as protection devices, amplifiers, switches, current limiters, oscillators, mixers, and voltage-controlled resistors.

3.2 Potential of 2D Materials in FET

Developments and advancements in materials have led to the exponential decrease in dimensions of the metal oxide semiconductor FET for over four past decades. This shrinking of size is the evidence of Moore's law prediction. These advancements not only scale down the size of silicon-based MOSFET but also enable it to perform even faster compared to its ancestors. However, this miniaturization and fast processing are possible at the cost of high-power consumption. This high-power requirement is due to the short-channel effect which arises in the MOSFET having a dimension less than 50 nm and makes the gate control weaken over the channel current. This results in disability of the gate to completely switch "off" the current through the channel [155]. This flow of unwanted leakage current, at the "switch off" state of MOSFET device, gives

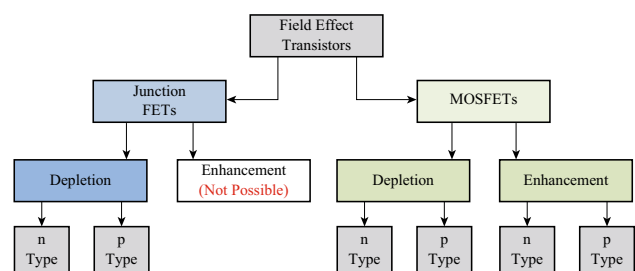


Fig. 3 FET tree

rise to the high-power consumption and overheating problems. Further miniaturization of MOSFETs has been restricted due to the aforesaid challenges. To mitigate these complications and have better gate control to completely prevent the current flow through the device at “off” state, different approaches such as multiple gates [155] and high- κ dielectric gate layer [156] have been investigated. However, tunneling field-effect transistor (TFET), another type of FET, in which carrier transport is due to the inter-band tunneling, can also show high $I_{\text{on}}/I_{\text{off}}$ with a low supply voltage which is attributed to the subthreshold slope (SS) <60 mV per decade [157, 158]. The potential of TFETs was first realized through the theoretical simulations [159, 160]. In addition, the research community is also looking for the alternate materials to complement or replace silicon technology. This brings the focus of researchers toward atomically thick mono or few layered 2D materials having unique characteristics appropriate for the future electronic devices, such as high mobility, transparency, and flexibility [161, 162]. The diverse properties of 2D materials, such as atomically thick body, robust nature, quantum confinement effect, high mobility, high switching efficiency, and tunable band gap, may result in the further scaling down of the device dimensions coupled with comparatively reduced short-channel effects [12, 21, 26, 30, 139]. In 2013, theoretical study, based on quantum transport simulations, shows promising results for reduction in channel length to ~ 10 nm [163]. Recently, experimental results, of U-shape MoS_2 FET with 10 nm channel length, have demonstrated excellent short-channel behaviors [164].

As described previously, 2D materials such as graphene and TMDC were fabricated from their bulk form due to the layered structure, which is held by a weak van der Waals force [1, 20] although good ohmic contact, higher carrier mobility, and band gap (~ 1 eV) are the basic requirements for any material to be used in logic applications such as MOSFET, cost-effective large-scale synthesis of the material, and its compatibility with CMOS technology are also of great importance [165]. Moreover, 2D TMDCs also possess large relative effective mass for electrons (~ 0.5) and holes (~ 0.66) compared to Si (~ 0.29) [166] which results in reduced source–drain tunneling component in case of TFETs [167]. Researchers are still working hard to search new high-performance 2D materials or improve the current 2D materials for the requirements. In the past decade, significant progress has been achieved in the field of 2D layered materials for the state-of-the-art electronic nanodevices. However, there is still no 2D material meeting all the requirements for the high-performance 2D-based electronic device. For example, graphene shows very high mobility [21] but lacks in switching efficiency (<10) at ambient temperature. On the other hand, MoS_2 has high

$I_{\text{on}}/I_{\text{off}}$ ratio (~ 108) [30] due to its relatively large band gap [26–28, 139] but has low electron mobility [30–32] compared to graphene. Many research works have shown that the number of the layers has a profound influence on the performance of electronic devices and the properties of layers can also be affected by the substrate or another 2D layered material coupled with them. Therefore, to form a heterostructure from two kinds of 2D materials, such as graphene and MoS_2 , may be employed to achieve and $I_{\text{on}}/I_{\text{off}}$ ratio simultaneously [4, 168]. Along with the aforesaid essential properties, thermal conductivity and heat dissipation are also of vital importance for the realization and thermal management of the high-quality electronic device. The theoretical and experimental studies of the thermal behavior of 2D TMDCs, despite being the promising materials for FET applications, are still limited as compared to graphene and h-BN [169–173]. However, thermal properties of monolayer MoS_2 (2D TMDC) differ from one-atom thin graphene layer due to its sandwich structure [174]. The thermal conductivity is mainly dominated by the phonons contribution rather than electrons [174]. Recently, theoretical investigations revealed the thermal conductivity of MoS_2 is 1.35 [175], 6 [176] or $23.2 \text{ W m}^{-1} \text{ K}^{-1}$ [174] in different reports, which is lower in the magnitude than that of graphene. Moreover, experimental studies of MoS_2 with a few layers have corroborated the thermal conductivity of 1.59 [177] and $52 \text{ W m}^{-1} \text{ K}^{-1}$ [178] at room temperature. Complete understanding of the thermal properties, of MoS_2 (TMDCs), is crucial for the future state-of-the-art electronic device applications.

Along with the experimental research, semiconductor-based FET modeling and simulation serve as a bridge between manufacturers and designers [179, 180] and provide essential tools to explore the fundamental properties of 2D TMDCs for the device applications [181]. Various softwares (such as PHILIPAC, SLIC, and SPICE) are available to model and investigate the devices [182, 183]. These compact models for TMDC-based FETs are vital to study the device behaviors with computational efficiency and accuracy without loss of the physical insights [184]. Before the industrial-level production of the integrated circuits of FET based on TMDCs, the study of devices using the compact model is of prime importance. Compact model for analyzing these devices differs from Si-based devices because of the Fermi–Dirac statistics and density of states’ effects on the capacitance [185–187]. Recently, many researchers have shown interest in developing the compact model for TMDC-based FETs. Each compact model has its own significance. For example, one model is based on capacitive network, which considers drift component but ignores trap effects [188]. Whereas, another model has more focus on the subthreshold region of the

device [189]. One of the models is developed to simplify the current and surface potential calculations with the help of the Boltzmann statistics [190]. Later on, the model is developed, for double-gate FETs, based on Fermi–Dirac statistics which involves implicit equations but excludes the trap effects [187]. The research work in [191] demonstrates the compact model, which also considered the Fermi–Dirac statistics with drift–diffusion transport. These models were developed to explore the behavior of the TMDC channel-based FETs.

3.3 Applications of 2D TMDC Materials in MOSFET

Metal oxide semiconductor field-effect transistors (MOSFETs) currently are the main components of any logic devices, and each digital circuit is composed of many logic gates. Any material chosen to be used in the fabrication of logic devices needs to satisfy some basic requirements such as low conductance at off condition to minimize the standby power consumption, high on/off switching ratio from 10^4 to 10^7 , and higher mobility of charge carrier for swift operation [192]. Large band gaps (1.2–2.5 eV) of bulk, few- or single-layered MoS_2 make it a suitable candidate to provide high switching ratio with low off-state power consumption [27, 28, 30]. Because of high switching

ratio and large band gap, MoS_2 being the potential candidate has been extensively studied for its application in the logic device. In this review, we will focus on MoS_2 -based FET as an example. Initially, low charge carrier mobility of $0.5\text{--}3\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, which is not sufficient for logic devices, was reported [29]. Subsequently, mechanically exfoliated nanopatches of MoS_2 exhibited a high on/off ratio $>10^5$ and charge carrier mobility in tens of $\text{cm}^2\text{ V}^{-1}\text{ s}^{-1}$ [193]. High switching on/off ratio of 10^8 , charge carrier mobility higher than $\sim 60\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, and subthreshold swing of 74 mV per decade (increase in gate voltage required to change the drain current by one decade. Here decade represents the 10 times increment in drain current) were reported in top-gated MoS_2 -based FET at room temperature [30–32]. Subthreshold swing gives the qualitative and quantitative analysis of $I_{\text{on}}/I_{\text{off}}$. A lower value of subthreshold swing for FET will result in higher $I_{\text{on}}/I_{\text{off}}$ and better switching behavior. At room temperature, the ideal subthreshold value is 60 mV per decade [13]. Similarly, monolayered MoS_2 FET has also shown on/off ratio of 10^8 and charge carrier mobility of $\sim 150\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ at 300 K once dielectric HfO_2 was used as the gate layer [30–33, 194] (Fig. 4).

MoS_2 showed low power consumption when high- k dielectric gate layer in top-gated configuration was used. Besides the high performance in FET, photoresponsivity in

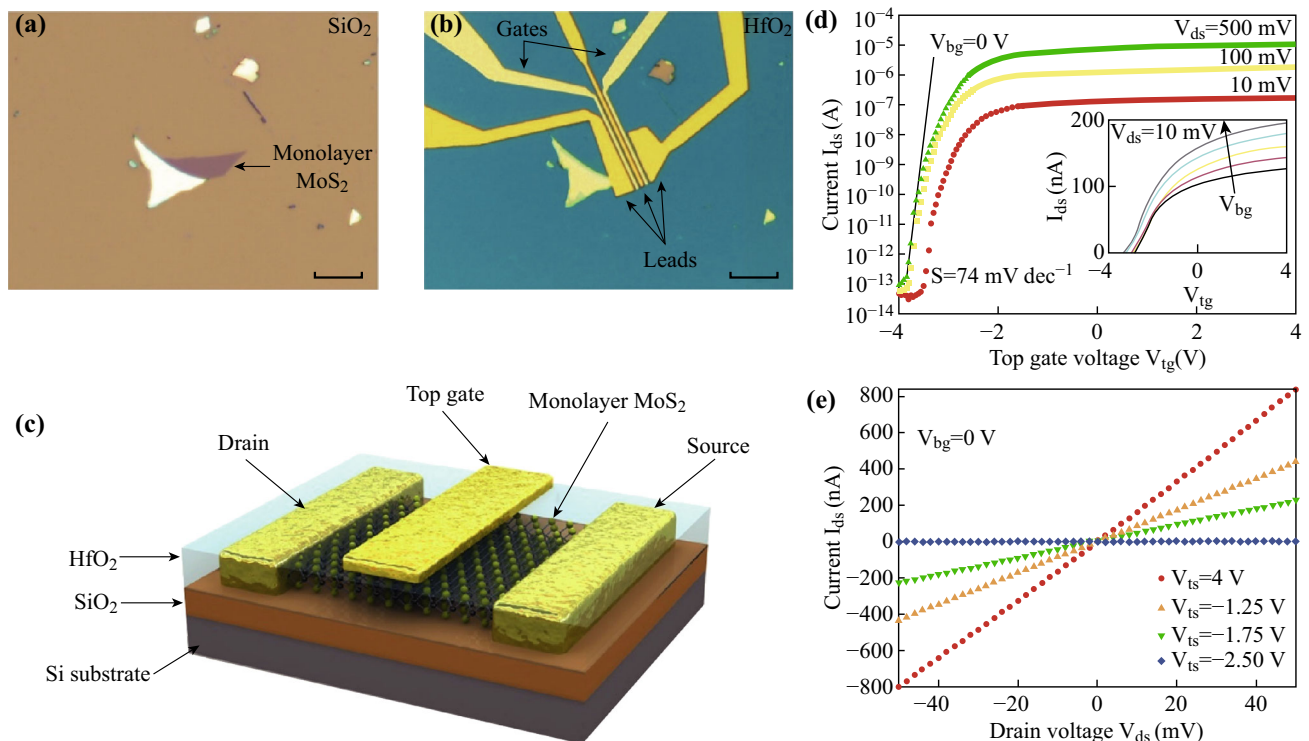


Fig. 4 a–c Preparation process of the single-layer MoS_2 transistor. d and e the gate control of single-layer MoS_2 transistor. Reprinted with permission from Ref. [30], Copyright 2011, Nature Publishing Group

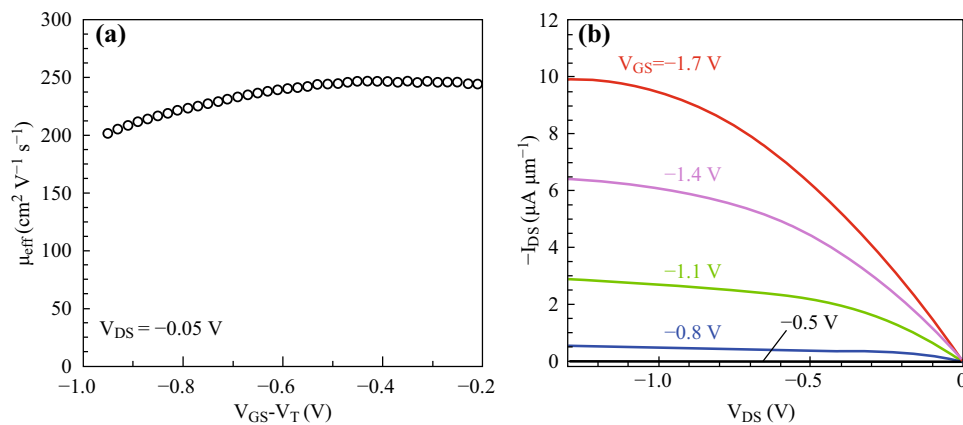


Fig. 5 **a** Effective hole mobility as a function of gate overdrive and **b** output characteristics of the *p*-type monolayer WSe₂ device. Reprinted with permission from Ref. [168], Copyright 2012, American Chemical Society

the range of 100–680 nm and ultrasensitivity of 880 A W^{-1} at a wavelength of 561 nm was observed in monolayered MoS₂ photodetectors [195]. The excellent optical properties of MoS₂ make it a potential material for the applications in video recording, optoelectronics, light sensing, and biomedical imaging applications [195–197]. Besides MoS₂, WSe₂, a *p*-type TMDC, is also equipped with the set of properties required for the device applications, such as considerable bulk indirect and monolayered direct band gap (1.2–1.65 eV) [198, 199]. FET based on bulk WSe₂ exhibited promising room-temperature hole (charge carrier) mobility of $\sim 500 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [200]. However, it lacked in on/off current ratio (>10). Bulk nature of WSe₂ results into large “OFF” state current which is not desirable for the efficient FET applications. In contrast, mechanically exfoliated single-layered WSe₂-based *p*-type FET has shown the hole mobility of $\sim 250 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ with the enhanced on/off current ratio ($>10^6$) and ideal subthreshold slope of ~ 60 mV per decade, as shown in Fig. 5 [199]. Moreover, *p*-type FET fabricated from CVD grown monolayer WSe₂ has demonstrated the hole mobility of $\sim 90 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ with an appropriate on/off current ratio of 10^5 [198, 201]. Similarly, MoTe₂-based FETs show the ambipolar response. Both *n*- and *p*-type material can be synthesized by controlling the growth method [202]. Theoretical calculations have depicted the room-temperature mobility of MoTe₂-based FET is of $\sim 200 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [203]. However, the recent experimental works for three-layered MoTe₂ device with Ti contacts have presented charge carrier mobility of 7×10^{-2} and $2 \times 10^{-2} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for holes and electrons, respectively [204, 205], whereas, in another work, a similar MoTe₂ device with Au contacts has shown improved mobility of $16.5 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ with on/off current of 10^7 [204].

Regarding the current research of TMDCs on FET, charge carrier mobility is the main focus. The impurities presented in mono or few layered MoS₂ material lead to screening effect, which influences the dielectric environment on charge carrier mobility. The large dielectric constant of the gate layer will increase the capacitive coupling between top gate and back gate which in return stimulates the charge carrier mobility by 10–50 times [194]. If only silicon/silicon dioxide is used as the substrate without high-*k* dielectric gate layer in mono or few layered MoS₂-based FET, charge carrier mobility of about $10 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ can be obtained at room temperature. Hence, the low mobility is due to the poor interface between Si/SiO₂ and MoS₂ [206, 207]. This interface problem including surface defects, the concentration of charged impurities, local charge distribution, and trapped charges in the substrate results in coulomb scattering and low charge carrier mobility. The use of high-*k* dielectric materials, such as hafnium dioxide (HfO₂) [30–32] or alumina (Al₂O₃) [208] as top gate, has increased the charge carrier mobility to ~ 150 and $500 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$, for monolayer and bulk MoS₂, respectively, due to the screening effect. Besides the influences of high-*k* dielectric gate layer and channel material (MoS₂) characteristics, charge carrier mobility has been underestimated due to the presence of Schottky barriers between metallic contacts and MoS₂ single or few layers [194, 209]. The reduction in resistance between the contacts and thinning of Schottky barrier results in an enhancement of charge carrier mobility from 100 to $220 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [210]. Theoretical calculations based on density function theory suggested that the carrier mobility of MoS₂ at room temperature could reach $400 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ [34]. These results suggest that MoS₂ is a promising material for future electronics.

4 Current Challenges in 2D Materials Device Application

Experimentally demonstrated charge carrier mobility of the mono or few layered MoS₂ is much lower than that of theoretical prediction of 410 cm² V⁻¹ s⁻¹ [34]. 2D materials possess large surface area making charge carrier mobility more sensitive to the external (e.g., trapped charged impurities, interface quality, and adsorbates from ambient air) and internal (lattice defects) factors [206, 207]. An experimental result of charge carrier mobility depends on the measurement condition/method and sample quality. Other factors including channel thickness, measuring temperature, annealing, Schottky barrier, dielectric environment, and carrier density (*n*) play an important role in achieving high charge carrier mobility devices.

The influence of channel thickness on carrier mobility was ascertained when mechanically exfoliated MoS₂ and NbSe₂ demonstrated 0.5–3.0 cm² V⁻¹ s⁻¹ charge carrier mobility, which is lower than their bulk counterparts [29]. Lee et al. [211] also showed the reduction in carrier mobility with the decrease in thickness placed on different substrates (SiO₂ and h-BN). One- to 5-layered MoS₂ displayed charge carrier mobility varying from 10 to 50 cm² V⁻¹ s⁻¹ [212]. The possible reasons for the thickness dependence are coulomb scattering and the Schottky barrier between channel and electrode contacts [213]. Moreover, in recent work, Hall mobility of ~1000 and ~34,000 cm² V⁻¹ s⁻¹ is reported for single- and six (6)-layered encapsulated MoS₂ devices, respectively, at a temperature below 5 K [214]. Just like the channel thickness, measuring or operating temperature has a significant effect on carrier mobility. High temperature (>100 K) enhances the lattice phonon scattering which tends to have an adverse effect on carrier mobility of 2D TMDCs. Consequently, the theoretically predicted charge carrier mobility of 410 cm² V⁻¹ s⁻¹ at room temperature [34, 215], limited by phonon scattering, has never been achieved experimentally for single-layered MoS₂ [216]. Similar behavior has also been reported for MoSe₂ with a few layers [217]. At low temperatures, high field-effect mobility (~1000 and ~34,000 cm² V⁻¹ s⁻¹) of single- and six-layered MoS₂ has been reported [214, 216]. Moreover, charge carrier density (*n*) also plays a vital role in electronic properties of 2D TMDCs materials. MoS₂ has shown electronic phase transition (metal to insulator) with an increase in charge carrier density [218, 219], whereas medium range charge carrier density is essential for the transistor applications. In this range, an increase in charge density may have two outcomes. First, high charge density is favorable for increasing carrier mobility by suppressing

the interfacial impurity potential. Second, high carrier density tends to increase the carrier energy which may result in reducing carrier mobility [212].

Interfacial Schottky barrier, between the channel semiconductor and metal electrodes, reduces the charge carrier mobility by inducing resistance in carrier transfer. This unwanted effect can be minimized by employing four-terminal measurement method [220]. Formation of the Schottky barrier is due to the difference in energy levels between the semiconductor and electrode materials. Schottky barrier height is directly proportional to the energy-level difference of two coupled materials [221]. Barrier height can be reduced by making contact between *n*-type semiconductor and low work function metals or *p*-type semiconductor and high work function metal. Moreover, the Schottky barrier is tunable by varying the FET gate bias. Initially, this variation was considered to be the switching mechanism of FETs [222]. Later, the dependence of barrier height on channel thickness was reported. In thicker flakes, the barrier height is much smaller than that of monolayered 2D TMDCs materials [223]. It is due to the influence of band gap of semiconductor channel on the Schottky barrier. Thinner (<5 layers) MoS₂ possesses larger band gap which results in higher barrier height and contact resistivity than bulk MoS₂ [220]. Barrier height between Au and MoS₂ varies from 0.3 to 0.6 eV with a decrease in the number of MoS₂ layers from 5 to 1 [220]. Hence, charge carrier mobility can be improved by optimizing the metal/semiconductor contact. Furthermore, minimum electrode length needs to be identified in order to obtain better charge transferring efficiency [220]. Channel length (in appropriately annealed samples), however, does not affect the MoS₂ device performance [220]. In addition, some studies have shown that the presence of ultrathin TiO₂ [224] or MgO [225], between MoS₂ and ferromagnetic metal, reduces interfacial Schottky barrier height.

Scattering in semiconductor channel is one of the reasons for the reduced charge carrier mobility. The scattering may be induced by lattice phonons due to the high-*k* dielectric environment, charged impurities, and interfacial phonons. At room temperature, bulk MoS₂ has exhibited the electron mobility ranging from ~150 to 500 cm² V⁻¹ s⁻¹ [30–33, 208]. However, if the monolayers of MoS₂ fabricated by mechanical exfoliated are transferred on SiO₂ to make a device, the carrier mobility then drops down to 0.1–10 cm² V⁻¹ s⁻¹ [29]. High charged impurity density (*N*) gives rise to coulomb scattering which can be screened with the use of high-*k* dielectric material, leading to the increase in electron mobility at low temperatures [219]. In FETs made of 2D TMDC materials, charged impurities (coulomb) are present at the interface between dielectric and 2D channel. These charged impurities have a

scattering potential which induces the scattering in 2D FETs [226–228]. The source of charged impurities includes chemical residues, adsorbates introduced during device fabrication, and contaminated surface, which results in reduced charge carrier mobility of the 2D TMDC-based FETs. Theoretical calculations and experimental results have demonstrated a high rate of coulomb scattering in the thinner channel with HfO_2 or SiO_2 as the gate layer [212], indicating that the top/bottom surface scattering is associated with channel thickness. As the thickness decreases, interaction distance between charge carriers and charged impurities shrinks due to the electrostatic equilibrium. This shrink in interaction distance results in high scattering potential and lower charge carrier mobility [212].

Charge carriers can be scattered by lattice phonons through potential deformation. Adjacent atoms move in the direction of acoustic phonons but opposite to the optical phonons. Phonon scattering is proportional to temperature and increases with the increase in temperature. Based on theoretical calculations (by the first principals calculations) of acoustic/polar phonon scattering and screening for single-layered MoS_2 , charge carrier mobility of $\sim 410 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ has been reported [215, 229, 230]. However, these calculations did not cater for the effects of dielectric mismatch and free-carrier screening. Phonon scattering becomes dominant due to the presence of high- k dielectric material and leads to a drastic decrease in electron mobility at room temperature (300 K) [230]. This phenomenon tends to increase as the thickness of the semiconductor layer is decreased from bulk to monolayer. In TMDC materials like MoS_2 , polar nature of the chemical bonds gives rise to the dipole moments between anions and cations. Perturbation of dipole moment by polar phonons creates an electric field which is coupled with charge carrier, resulting in low charge carrier mobility. This phenomenon is called Frohlich interaction or polar optical phonon scattering [229]. Phonons can be excited by the charge carriers if the dielectric layer in FETs supports polar vibrational modes. These phonons are known as surface optical phonons or remote interface phonons. At room temperature, scattering due to remote interface phonons is more dominant in the high- k dielectric environment compared to low k dielectric gate layer [231, 232].

Besides coulomb and phonon scattering, structural defects also play a vital role in the degradation of charge carrier mobility. Structural defects include dislocation, vacancies, grain boundaries, impurities, and precipitation. In a low-quality sample, anion vacancies can act as a strong scattering source. Studies have shown that CVD grown or mechanically exfoliated MoS_2 possesses high percentages (0.4%) of sulfur vacancy which affects the charge carrier mobility [233]. Vacancy repairing of CVD grown single-

layer MoS_2 by annealing can improve the charge carrier mobility up to $45 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [234]. Vacancy scattering is independent of carrier density and weakly depends on the temperature and channel thickness as these parameters do not have any direct relation with the defect densities [235]. Besides vacancy defects, the presence of tilt grain boundaries may also degrade the charge carrier transport efficiency [236].

Electron or charge carrier density (n) is also one of the factors affecting the charge carrier mobility. Although electron mobility tends to increase with the increase in electron density, the effect is prominent after the effective screening of phonon scattering. As the dielectric value of k increases, electron mobility drastically decreases due to phonon scattering. Electrons presented in atomically thick 2D mono or few layer nanosheets excite the phonons in the nearby dielectric material (which supports polar vibrational modes) at room temperature. Figure 6a [230] demonstrates the effects of dielectric environment on charge carrier mobility at two different temperatures of 100 and 300 K. In both cases, electron density and charged impurity density are considered equal to 10^{13} cm^{-2} . The solid line represents the combined effects of coulomb and phonon scattering on mobility, whereas the broken line shows the electron mobility while neglecting the effects of phonon scattering, which indicates a trend to achieve large mobility at high- k dielectric environment (ϵ_c). In this case, mobility is entirely dependent upon the charged impurity density.

At low temperature, when the phonon scattering is inactive and negligible, electron mobility can be improved by decreasing the charged impurity density. If the charged impurities density is low, low k dielectric is required for coulomb screening, which will result in less phonon scattering at room temperature [230]. Figure 6b [230] shows the dielectric constant required against the critical value of charged impurity density N_{cr} at room temperature. If $N > N_{\text{cr}}$, then the electron mobility highly depends upon N rather than phonon scattering and vice versa. Figure 6c [230] represents the charge carrier mobility of a monolayer MoS_2 (phonon limited) at room temperature under different dielectric environment ranging from free suspension in the air to high- k dielectric HfO_2 . It can be inferred from the plot that the phonon determined mobility decreases with the increase in dielectric constant of the gate layer. Figure 6d [230] demonstrates the combined room-temperature electron mobility in monolayer MoS_2 nanosheet against variable charged impurity densities under various dielectric environments considering all kinds of scattering mechanisms. The carrier density is fixed to be 10^{13} cm^{-2} . From Fig. 6d, one can figure out that the electron mobility is weakly dependent on the dielectric environment at high impurity density (10^{13} cm^{-2}), as shown in the dashed box in the bottom right corner.

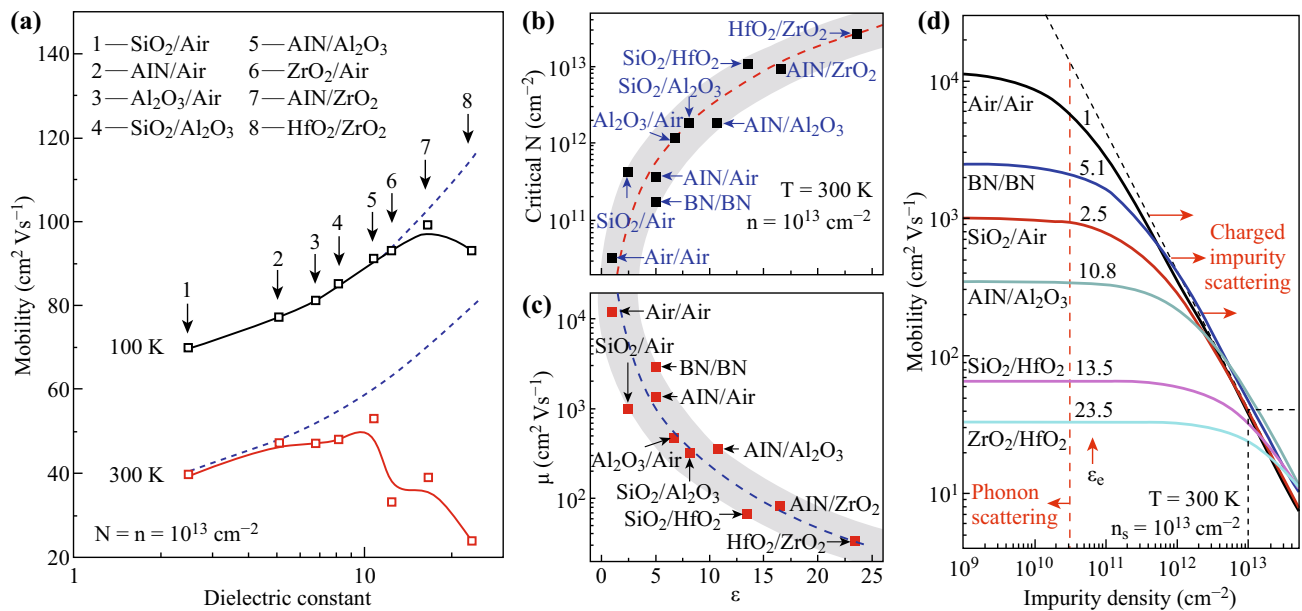


Fig. 6 **a** Electron mobility as a function of dielectric constant. Dashed lines show the mobility without considering the SO phonons. **b** The critical impurity densities N_{cr} and **c** Room-temperature electron mobility in monolayer MoS₂ surrounded by different dielectrics. **d** The room-temperature net electron mobility in monolayer MoS₂ considering all kinds of scattering mechanisms as a function of impurity density (N). Reproduced from Ref. [230]

5 Future Prospective and Conclusion

Aforementioned challenges, regarding the utilization of 2D nanomaterials in device applications in connection with the charge carrier mobility, drive us not only to produce the high-quality (defect- and impurity-free) single-crystal mono or 2D nanosheets with a few layers but also to think about searching new materials. This path leads to two methodologies pertaining to the improvement of charge carrier mobility by the utilization of existing materials via special design, such as heterostructure technique or experimental study of some new materials, which is possible to have high carrier mobility.

For the first methodology, efforts need to be made to produce the high-quality and defect-free 2D nanostructure which contains a minimum level of charged impurity density. Mechanical exfoliation can produce high-quality TMDCs. However, the difficulty for large-scale synthesis with uniformity and reproducibility of samples are the main limitations of this process. CVD is a method which has the potential of producing the large-scale high-quality 2D TMDCs or graphene [237, 238]. In order to obtain the impurity-free high-quality 2D materials, the ultraclean substrate (flushing of the substrate with acetone and isopropanol and subsequently vacuum annealing at high temperature) and highly pure precursors need to be used. In addition, the synthesis parameters such as pressure, temperature, and growth time are needed to be optimized, which are all important to achieve large-scale, high-quality

single-crystal 2D materials [237–239]. Proper procedures to avoid contamination during 2D material synthesis are also of importance. For example, the purging of Ar gas with a very high purity is required to eliminate any chance of impurity in the samples [240]. Thickness and number of layers of 2D material can be controlled by controlling the deposition parameters, such as heating temperature, deposition time, and chamber pressure [238, 241]. Furthermore, very recent developments have shown that adding a small amount of O₂ in the Ar carrier gas can also suppress the nucleation and promote the synthesis of MoS₂ with a large area and high quality [239]. In addition, device fabrication and encapsulation inside Ar-filled glove box will also help avoid device degradation, possibly due to the presence of chemical species (e.g., O₂ and H₂O) in ambient condition [242].

From the above discussions, charge carrier mobility in 2D materials is primarily dependent on the concentration of the charged impurities and then on the phonon scattering due to the dielectric environment at high temperatures. CVD method has the potential to generate high-quality large-scale single-crystal 2D nanosheets. MoS₂, graphene, WS₂, and MoTe₂ high-quality monolayers have been extensively reported using CVD techniques. Recently, it has been observed that assembling different 2D materials into heterostructure may lead to the tuning of electronic properties [243, 244]. A band gap of 0.1 eV of MoS₂ was achieved after a heterostructure composed of MoS₂, and graphene was formed [243]. Furthermore, heterostructure-

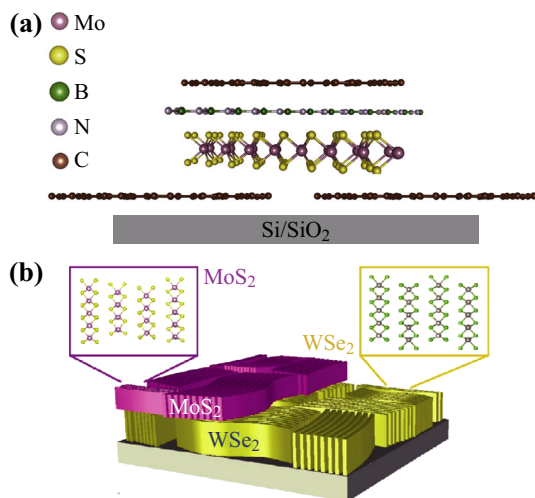


Fig. 7 Heterostructure-based **a** FET composed of MoS₂ (channel), h-BN (top-gate dielectric), and graphene (source, drain, and top-gate electrodes). Redrawn from Ref. [245] and **b** p–n junction fabricated from vertical stacked MoS₂ (*n* type) and WSe₂ (*p* type). Reprinted with permission from Ref. [247]. Copyright (2015) American Chemical Society

based FET composed of MoS₂ (channel), h-BN (top-gate dielectric), and graphene (source, drain and top-gate electrodes) has displayed charge carrier mobility of $\sim 33 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and on/off current ratio of $>10^6$ [214, 245] (Fig. 7a). Besides MoS₂, TMDCs p–n junction (heterostructure) also demonstrates promising results. Heterostructure of TMDCs, n-MoSe₂/p-WSe₂, has exhibited the clear rectification with an ideality factor of ~ 2 at 290 K [246]. Similarly, p–n junction of p-WSe₂/n-MoS₂ (Fig. 7b) has also shown the promising gate tunable rectifying electrical characteristics [247–250]. The average conductance slope of 75 mV per decade at room temperature [250] and ideality factor of 1.2 were observed [251]. However, in recent work, the p–n heterojunction formed by *p*-type single-walled carbon nanotubes and *n*-type monolayer MoS₂ has also revealed the charge transport behavior with a forward/reverse current ratio of larger than 10^4 [252]. In addition, heterostructure made from InAs (*n* type)/WSe₂ (*p* type) has displayed the even better rectification with a forward/reverse current ratio larger than 10^6 and an ideality factor of ~ 1.1 [253].

Secondly, to search and fabricate new materials may be another possible methodology to achieve high carrier mobility 2D materials. Recently, 2D material, InSe (metal chalcogenide)-based heterostructure encapsulated device has been reported, which demonstrates charge carrier mobility of $\sim 10,000$ and $\sim 1000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ at ~ 50 and 300 K, respectively [242]. Theoretical calculations have revealed that some new promising single-layer 2D TMDC materials may achieve higher mobility than that of

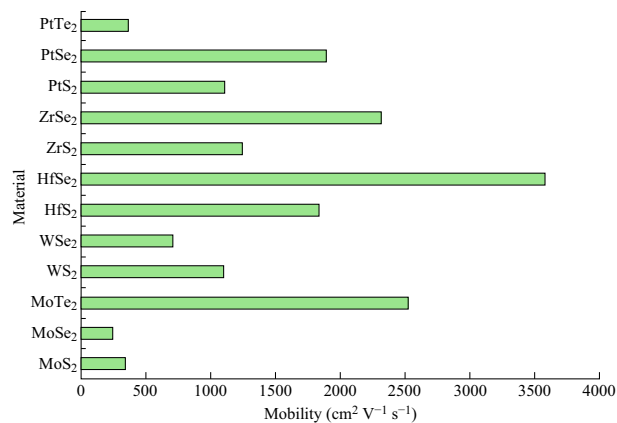


Fig. 8 Theoretical charge carrier mobility of monolayer 2D TMDC materials. Redrawn from Ref. [254]

MoS₂ [254] as shown in Fig. 8. Certainly, the synthesis of these high-quality 2D materials is a challenge.

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